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**Dynamic Characteristics of Grid-Connected Three-Phase
Z-Source Inverter in Photovoltaic Applications**



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ABSTRACT

Due to the inevitable depletion of fossil fuels and increased awareness of their harmful environmental effects, the world energy sector has been moving towards extensive use of renewable energy resources, such as solar energy. In solar photovoltaic power generation, the needed interface between the source of electrical energy, i.e., a photovoltaic generator, and electrical energy transmission and distribution systems is provided by power electronic converters known as inverters. One of the latest addition into the large group of inverter topologies is a Z-source inverter (ZSI), whose suitability for different applications have been extensively studied since its introduction in 2002. This thesis addresses the dynamic characteristics of a three-phase grid-connected Z-source inverter when applied to interfacing of photovoltaic generators. Photovoltaic generators have been shown to affect the behavior of the interfacing power converters but these issues have not been studied in detail thus far in case of ZSI.

In this thesis, a consistent method for modeling a three-phase grid-connected photovoltaic ZSI was developed by deriving an accurate small-signal model, which was verified by simulations and experimental measurements by means of a small-scale laboratory prototype inverter. According to the results presented in this thesis, the small-signal characteristics of a photovoltaic generator-fed and a conventional voltage-fed ZSI differs from each other.

The derived small-signal model was used to develop deterministic procedure to design the control system of the inverter. It is concluded that a feedback loop that adjusts the shoot-through duty cycle should be used to regulate the input voltage of the inverter. Under input voltage control, there is no tradeoff in between the parameters of the impedance network and impedance network capacitor voltage control bandwidth. Also the small mismatch in the impedance network parameters do not compromise the performance of the inverter. These phenomena will remain hidden if the effect of the photovoltaic generator is not taken into account. In addition, the dynamic properties of the ZSI-based PV inverter was compared to single and two-stage VSI-based inverters. It is shown that the output impedance of ZSI-based inverter is similar to VSI-based inverter if the input voltage control is designed according to method presented in the thesis. In addition, it is shown that the settling time of the system, which determines the maximum power point tracking performance, is similar to two-stage VSI-based inverter.

The control of the ZSI-based PV inverter is more complicated than the control of the VSI-based inverter. However, with the model presented in this thesis, it is possible to guarantee that the performance of the inverter resembles the behavior of the two-stage VSI, i.e. the use of ZSI in interfacing of photovoltaic generators is not limited by its dynamic properties.

PREFACE

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SYMBOLS AND ABBREVIATIONS

Abbreviations

AC, ac	Alternating current
AD	Analog-to-digital conversion
CC, cf	Constant-current
CF, cf	Current-fed
CSI	Current-source inverter
CV, cf	Constant-voltage
CCM	Continuous conduction mode
DA	Digital-to-analog conversion
dB	Decibel
dc	Direct current
DSP	Digital signal processor
ESR	Equivalent series resistance
FPGA	Field-gate-programmable array
IGBT	Insulated gate bipolar junction transistor
LHP	Left half plane
NPC	Neutral-point clamped
MPP	Maximum power point
MPPT	Maximum power point tracking
OC	Open-circuit
PI	Proportional-integral controller
PLL	Phase-locked loop
PV	Photovoltaic
PVG	Photovoltaic generator
PWM	Pulse-width modulation
RHP	Right half plane
SC	Short-circuit
STC	Standard-test conditions
VF, vf	Voltage-fed
VSI	Voltage-source inverter
ZSI	Z-source inverter

Greek characters

α	Alpha-component in stationary reference frame
β	Beta-component in stationary reference frame
Δ	Determinant, difference
ω	Angular frequency
θ	Vector angle
Φ	State-transition matrix

Latin characters

a	Diode ideality factor
A	Coefficient matrix of the state-space representation
B	Coefficient matrix of the state-space representation
B	Boost factor
C	Coefficient matrix of the state-space representation
c	Control variable
C_1, C_2	Impedance network capacitance
C_{in}	Input capacitor impedance
C_{dc}	Dc-link capacitance
d	Differential operator
D, d	Duty ratio
D', d'	Complement of the duty ratio
D	Coefficient matrix of the state-space representation
f	Frequency
G	Transfer function matrix
G_{ci}, \mathbf{G}_{ci}	Control-to-input transfer function
G_{co}, \mathbf{G}_{co}	Control-to-output transfer function
G_{czc}	Control-to-impedance network capacitor voltage transfer function
G_{io}, \mathbf{G}_{io}	Forward transfer function
G_{izc}	Input-to-impedance network capacitor voltage transfer function
G_{ozc}	Output-to-impedance network capacitor voltage transfer function
I	Identity matrix
i_{pv}, I_{pv}	Photovoltaic generator current
i_{ph}, I_{ph}	Photocurrent
i_d, I_d	Diode current
i_{in}	Input current
\hat{i}_{in}	Perturbed input current
i_o	Output current
$\hat{i}_o, \hat{\mathbf{i}}_o$	Perturbed output current
i_{dc}	Dc-link current
\hat{i}_{dc}	Perturbed dc-link current
I_0	Diode reverse saturation current

k	Boltzmann constant
L	Inductance, loop-gain
N_s	Number of series connected cells
q	Elementary charge
r_{pv}	Dynamic resistance of a photovoltaic generator
R_{pv}	Static resistance of a photovoltaic generator
R_{sh}	Shunt resistance of a PVG
R_s	Series resistance of a PVG
r_D	Diode on-stage resistance
r_{sw}	Transistor on-stage resistance
r_C	Parasitic resistance of a capacitor
r_C	Parasitic resistance of an inductor
s	Laplace variable
S	Switch
T_d	Time delay
T	Temperature
T_{oi}, \mathbf{T}_{oi}	Reverse transfer function
\mathbf{u}	Input variable vector
u_{pv}, U_{pv}	Photovoltaic generator voltage
\hat{u}_{pv}	Perturbed photovoltaic generator voltage
u_o	Output voltage
$\hat{u}_o, \hat{\mathbf{u}}_o$	Perturbed output voltage
u_{Cz}	impedance network capacitor voltage
\hat{u}_{Cz}	Perturbed impedance network capacitor voltage
u_{dc}	Dc-link voltage
\hat{u}_{dc}	Perturbed dc-link voltage
u_{in}	Input voltage
\hat{u}_{in}	Perturbed input voltage
U_D	Diode forward voltage drop
v_c	PWM control signal
\mathbf{x}	State variable vector
\mathbf{y}	Output variable vector
Y_{in}	Input admittance
Y_o, \mathbf{Y}_o	Output admittance
Z_{in}	Input impedance
Z_o, \mathbf{Z}_o	Output impedance

Subscripts

c	Error amplifier, controller
d	Direct component
q	Quadrature component

lf	low-frequency
st	shoot-through
conv	Refers to the control system reference frame
grid	Refers to the synchronous reference frame
inf	Refers to ideal transfer function

Superscripts

cf-in	Refers to transfer functions of current-fed impedance network
vf-in	Refers to transfer functions of voltage-fed impedance network
in	Refers to transfer functions of an input voltage-controlled converter
T	Transpose
out	Refers to transfer functions of an output current-controlled converter
S	Refers to source affected transfer functions
vsi	Refers to transfer functions of VSI
zsi	Refers to transfer functions of ZSI

1 INTRODUCTION

This chapter provides an introduction to the thesis by first discussing on the role of power electronics in the interfacing of distributed generation units, such as solar photovoltaic power plants, into a power system. After that the fundamental operation of photovoltaic devices and the common system configurations used in solar photovoltaic power systems are reviewed. This chapter also introduces the Z-source inverter (ZSI) for the grid-interfacing of the photovoltaic generators. Finally the scientific contributions of the thesis are summarized.

1.1 Role of power electronics in energy production

Modern society is driven by electricity: e.g. transportation, manufacturing processes, heating, lighting, and consumer electronics consume large amount electrical energy. For decades, the source of electrical energy has been the large concentrated power plants, where synchronous generators are utilized to convert the fundamental source of energy (e.g. coal, oil, peat, potential energy of water) to electrical energy. The torque rotating the synchronous generators is provided most often by steam generator or water-turbine. However, regardless of the real source of energy, the traditional electrical energy production does not require power electronics.

Inevitable depletion of fossil fuels and increased awareness on their environmental effects have turned the focus of energy sector towards extensive utilization of renewable energy resources such as wind and solar energy. Especially, the solar energy has been observed to be one of the most promising alternative for fossil fuels (Romero-Cadaval et al.; 2013) and (Kouro et al.; 2015). Solar energy can be harnessed in two ways: First, solar thermal technologies utilize sunlight to heat water for domestic usage, warm building spaces, or heat fluids to drive electricity-generating turbines. Second, photovoltaic generators (PVGs) are semiconductor devices that convert sunlight directly to electricity through photovoltaic (PV) effect. In the grid-connected system, the direct current generated by the PV devices is converted to ac and fed directly to the grid using power electronic converters known as inverters. Grid-connected PV systems account for more than 99 % of the PV installed capacity compared to stand-alone systems (Kouro et al.; 2015).

The installed solar photovoltaic capacity has increased enormously during the last years. According to the report published by International Energy Agency (IEA) in early 2015 , around 177 GW of PV have been installed globally by the end of 2014, at least 10 times higher than in 2008 (International Energy Agency; 2015). As a result, at least 200 TWh will

be produced in 2015 by PV systems installed and commissioned until January 2015. This represents about 1 % of the electricity demand of the Earth, although some countries have reached even more significant percentages (e.g. Italy, Greece and Germany over 7 %). The Institute of Electrical and Electronics Engineers (IEEE) has ambitious prediction that, by 2050, PV will supply 11 % of the global electricity demand (Bose; 2013).

Efficient energy production using PV is not possible without power electronics, which provides the needed interface between the three-phase power transmission network and photovoltaic generators. The same principles apply also for wind-power plants and fuel-cell applications, where the power electronics are required to optimize the energy production (Blaabjerg et al.; 2004). However, since the solar energy (and wind energy) are intermittent by nature, a large regulating system is required when the amount of renewable energy resources increases. The regulating system may include energy storage or small conventional power plants.

According to the estimate of the Electric Power Research Institute, approximately 70 % of electrical energy consumed in the USA flows through power electronics (Bose; 2013). These power electronics driven loads include e.g. frequency converters, compact fluorescent lamps, LEDs, heat pumps, and power supplies. More than likely similar transition will be observed in the production of electrical energy, since the number of grid-connected power-electronics based power generation will increase significantly in the future changing the traditional system into a distributed system, where the production and the control of the power system is distributed (Liserre et al.; 2010) (Divan et al.; 2014) (von Appen et al.; 2013).

1.2 Overview of solar photovoltaic power systems

Photovoltaic (PV) devices convert sunlight directly into electricity based on the photovoltaic effect first observed by French physicist A. E. Becquerel in 1839. The basic building block of a PV device is a solar cell. A set of series-connected cells form a PV module and a set of series or parallel connected modules form a PV array. In general, the PV device is known as a photovoltaic generator (PVG).

Operation of PV cells and modules

The most common solar cell is a large-area p-n junction made from silicon, i.e. PV cell is a diode that is exposed to light. The photovoltaic phenomenon inside the p-n junction can be summarized as the absorption of solar irradiation, the generation and transport of free carriers and collection of these electric charges at the terminals of the cell. The rate of generation of electric carriers depends on the flux of incident light. According to (Villalva et al.; 2009), the static electrical terminal characteristics of a PV cell can be represented by a single-diode model depicted in Fig. 1.1. A current source I_{ph} describes the current generated by the incident light and a non-ideal diode represents the p-n junction inside the cell. Resistive losses R_s and R_{sh} are included in the model to take into account the different terminal ohmic losses. Since the PV module or array is a combination of series and/or parallel-connected single PV cells, their current-voltage characteristics in uniform environmental conditions can be represented

also by using the single-diode model. According to Shockley diode equation, the terminal current of a PV cell can be given by:

$$I_{pv} = I_{ph} - \underbrace{I_0 \left[\exp \left(\frac{U_{pv} + R_s I_{pv}}{N_s a k T / q} \right) - 1 \right]}_{I_d} - \frac{U_{pv} + R_s I_{pv}}{R_{sh}}, \quad (1.1)$$

where I_{ph} is the current generated by the incident light, I_0 is the diode reverse saturation current, N_s is the number of series connected cells, a is the diode ideality factor, T is the absolute temperature, k is the Boltzmann constant, and q is the elementary charge.

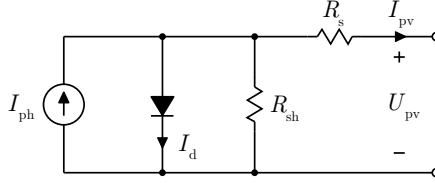


Figure 1.1. Single-diode model of a photovoltaic generator.

Typical non-linear current-voltage and power-voltage characteristics of the PVG is illustrated in Fig. 1.2. The three operating points, usually used to characterize the I-V curve, are known as a short-circuit (SC), an open-circuit (OC), and a maximum power point (MPP). According to (1.1), the temperature increase will decrease the open-circuit voltage and the increase in the solar irradiation will increase the open-circuit current. The power of a PVG is maximized usually during the spring, when the temperature is still low and irradiation is high. PV-module datasheet generally gives information on the characteristics and performance with respect to the so-called standard test condition (STC), which corresponds to an irradiation of 1000 W/m^2 at 25°C . Datasheet parameters can be used to derive the single-diode-model parameters by utilizing the methods presented e.g. in (Chatterjee et al.; 2011) and (Ding et al.; 2012).

The current-voltage characteristics, depicted in Fig. 1.2, clearly indicates that the photovoltaic generator differs significantly from the traditional voltage sources, such as a battery. It has properties both of a voltage source and a current source depending on its operating point. When the voltage of the generator is lower than the MPP voltage, the PVG behaves as a current source. When the voltage of the generator is higher than the MPP voltage, it behaves as a voltage source. At maximum power point, the behavior resembles a constant power source.

Interfacing power electronic converters

In a three-phase grid-connected photovoltaic system, the inverter interfacing the photovoltaic generator must produce a three-phase current that is correctly synchronized with the grid voltage. Today, the control objective of the inverter is to operate at a power factor close to unity and set operating point of the PVG at the maximum power point. These systems are known as maximum-power-point tracking PV inverters (Blaabjerg et al.; 2006). Depending

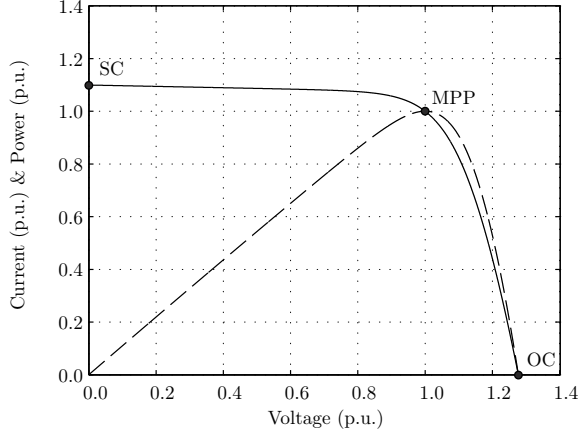


Figure 1.2. Typical non-linear static current-voltage (solid line) and power-voltage (dashed line) characteristic of a photovoltaic generator.

on the location, the inverters are required to perform also several auxiliary functions such as reactive power injection (var compensation), inertial response, and maximum power tracking (Sangwongwanich et al.; 2015).

Traditionally, three-phase inverters are categorized based on the voltage levels at the input (dc) and output (ac) terminal. Voltage-buck-type inverter requires that the input voltage is higher in magnitude than the amplitude of the line voltage at the inverter output terminals. In voltage-boost-type inverter, the input voltage must be lower in magnitude than the amplitude of the line voltage. The widely used voltage-buck-type PV inverter, shown in Fig. 1.3a, is based on a voltage source inverter (VSI), and the voltage-boost-type PV inverter, shown in Fig. 1.3a, is based on a current source inverter (CSI). Three-phase VSI-based PV inverter can be equipped with a voltage-boosting dc-dc stage that will increase the input voltage range of the power converter (Femia et al.; 2009), (Meneses et al.; 2013). This configuration, also known as two-stage inverter, is illustrated in Fig. 1.4.

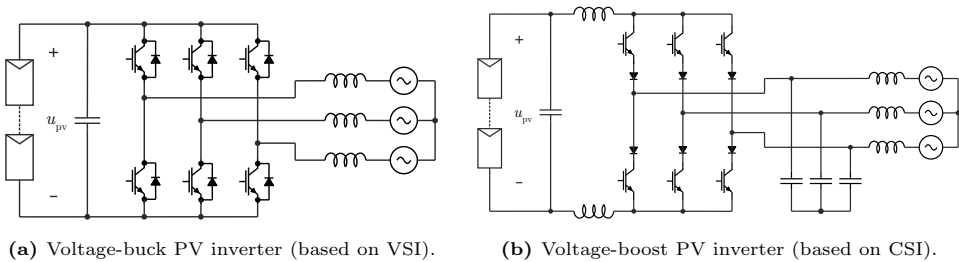


Figure 1.3. Two most common three-phase single-stage inverter structures.

Blaabjerg et al. (2004), Kjaer et al. (2005), Carrasco et al. (2006), and Araújo et al. (2010) have classified the grid-connected PV inverters based on the ac and dc-side connection topology. The concepts are illustrated in Fig. 1.5. The module-integrated concept is used to

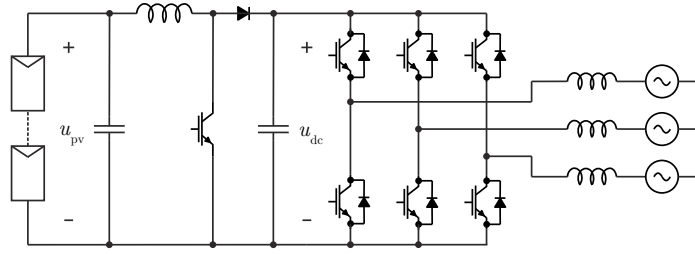


Figure 1.4. Three-phase two-stage photovoltaic VSI.

connect a single module to single-phase system, where a dc-dc voltage-boosting stage is used to provide high enough dc-side voltage for the dc-ac conversion stage. In string concept, a large amount of PV modules is connected in series to provide high enough voltage to the inverter. Traditionally string inverters have been single-phase devices but the amount of three-phase products have been steadily increasing. In multi-string and central inverter concept, a three-phase device is often preferred.

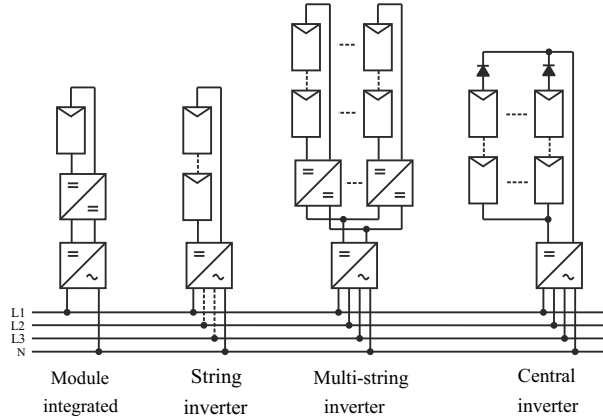


Figure 1.5. Grid interfacing (redrawn from Kjaer et al. (2005))

Maximum power-point tracking and partial shading of PVG

The photovoltaic generator should be operated at maximum power point to maximize the energy yield. The maximum power point tracking (MPPT) is implemented in the interfacing power electronic converter. The PVG current dramatically varies with irradiation and easily saturates the control system (Xiao, Dunford, Palmer and Capel; 2007), whereas the MPP voltage is mainly affected by the slowly changing temperature, i.e. the regulation of the PVG voltage results in a better performance than regulating the PVG current. The most common MPPT-methods are perturb and observe (P&O) and incremental conductance (IC) (de Brito et al.; 2013). The P&O method operates by periodically incrementing or decrementing the terminal voltage of the PVG and comparing the power obtained in the current cycle with the power of the previous one (Kjaer; 2012). The IC method is based on the fact that

the slope of the current-voltage curve, i.e. the dynamic resistance, corresponds to the static resistance of the PVG at the maximum power point (Kjaer; 2012).

Commercial PV modules typically contains 30 to 60 series connected PV cells. Modules are usually equipped with bypass diodes to prevent the cells from overheating and to increase their power production when they are partially shaded. Without the bypass diodes the current of the whole PVG is limited by the shaded cell. Fig. 1.6 shows I-V and P-V curves of module having three bypass diodes when one third of the surface is shaded. According to Fig. 1.6, the PV module has multiple maximum power points when it is partially shaded. The number of maximum power points equals to the number of bypass diodes and only one of the maximum power points is the global maximum (Nguyen and Low; 2010). As shown in Fig. 1.6, the voltage of the global maximum power point might be lower than in normal conditions and might be unreachable for the interfacing converter.

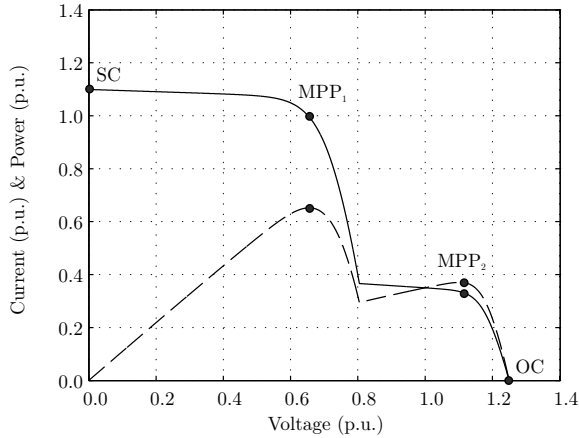


Figure 1.6. Typical non-linear static current-voltage (solid line) and power-voltage (dashed line) characteristic of a photovoltaic generator. One of the three modules is receiving one third of the irradiation of the others.

The problems associated with the nonuniform environmental conditions have been addressed several ways. In distributed MPPT, each PV module or string has own power converter that enables optimization of the power production (Xiao, Ozog and Dunford; 2007) (Femia et al.; 2008), which naturally decreases the number of maximum power points during the partial shading conditions. Also methods that reconfigures the series/parallel connections of PV modules in large PV array have been proposed (Velasco-Quesada et al.; 2009) (Lavado Villa et al.; 2013). In addition, it has been demonstrated that a parallel connection of PV cells does not suffer shading problems but requires power converter with a high voltage gain and high input current capability (Gao, Dougal, Liu and Iotova; 2009).

1.3 Z-source inverter (ZSI)

Z-source inverter (ZSI) has been introduced by F. Z. Peng in 2002 showing several advantageous characteristics over the classical VSI and CSI topologies (Peng; 2002), (Peng; 2003). The most significant advantage of the converter is its buck/boost property, which allows wide input voltage range without any additional power processing stage. This makes the converter highly suitable for module integrated and string inverters, where the wide input voltage range together with a large voltage-gain are highly desired properties. Other advantages of the converter is the lack of deadtime requirement in switch matrix control, which reduces low-order harmonics produced by the inverter bridge (Liu, Haitham and Ge; 2014).

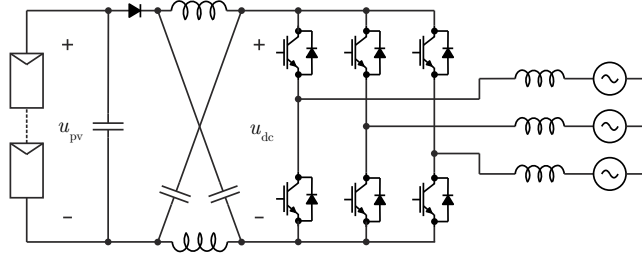


Figure 1.7. Three-phase ZSI-based photovoltaic inverter.

The main circuit diagram of the ZSI suitable for enabling three-phase grid-interfacing of photovoltaic generators is depicted in Fig. 1.7. Contrary to the original circuit diagram presented in (Peng; 2002), the power circuit is equipped with an input capacitor and a grid-interfacing three-phase inductor. These filter structures are required to provide continuous current and power flow at the input and output terminal as discussed in (Huang et al.; 2006). Most often, and as in Fig. 1.7, the traditional two-level VSI-type switch matrix is utilized in the ZSI since they are widely commercially available. However, it is also possible to use a three-level NPC bridge as discussed in (Loh et al.; 2006) and (Loh, Lim, Gao and Blaabjerg; 2007) or a CSI-type bridge as discussed e.g. in (Loh, Vilathgamuwa, Gajanayake, Wong and Ang; 2007).

Since the introduction of the original Z-source inverter in 2002, numerous derivatives of the basic converter have been proposed. Quazi-Z-source inverter (Anderson and Peng; 2008) provides similar properties as the traditional ZSI but the impedance-network-capacitor-voltage stress is reduced. In the embedded Z-source inverter, the dc-source is inserted in parallel with the impedance network capacitor (Gao et al.; 2008), and in the series Z-source inverter (also known as the improved Z-source inverter) (Tang et al.; 2011), the impedance network is connected in series between the source and the inverter bridge. In addition, numerous impedance networks based on utilizing transformer or coupled inductors have been proposed (Qian et al.; 2011) (Loh et al.; 2013) (Siwakoti, Blaabjerg and Loh; 2015). A comprehensive overview of different topologies is presented e.g. in (Siwakoti, Peng, Blaabjerg, Loh and Town; 2015). It should be noted that in addition to impedance source inverters, there are numerous other inverter topologies that can operate in buck and boost modes. These include e.g. Sepic, Zeta,

and Ćuk-converter-based inverters (Kikuchi and Lipo; 2002), switched boost (Upadhyay et al.; 2011), and diode assisted voltage-source inverter (Gao, Loh, Teodorescu and Blaabjerg; 2009).

Fundamentally, the ZSI operates as two-stage VSI, where the dc-link and the PVG voltage can be controlled independently. The voltage-boosting property of the ZSI is achieved by inverter bridge shoot-through state that will alter the impedance network capacitor charge and inductor flux-linkage balances. To include the required shoot-through state inside the modulation period of the inverter bridge, numerous different conventional (Loh et al.; 2005) and space-vector-based (Liu, Ge, Abu-Rub and Peng; 2014) pulse-width modulation schemes have been developed for the ZSI. The modulation method affects the ripple in the impedance network inductor current (Shen et al.; 2006), the ripple in the capacitor voltage (Hanif et al.; 2011), the voltage stress of the components (Peng et al.; 2005), and the leakage current (Bradaschia et al.; 2011). When the ZSI operates in voltage-buck mode, the impedance network operates as an additional input filter and the same modulation methods as in VSI-type inverter can be directly utilized.

As in the two stage inverter, the steady state value of the equivalent dc-link voltage can be chosen arbitrary as long as it is higher than the amplitude of the grid line voltage and the required shoot-through states can be inserted inside the modulation period. To minimize the losses, the voltage should be as low as possible. However, due to the insertion of the shoot-through states, the equivalent dc-link voltage (i.e. input voltage of the switching bridge) must be increased when the ZSI operates in voltage-boosting mode. As a result, the ZSI efficiency drops significantly when low input voltage is used (Wei et al.; 2011). The use of three-level bridge can significantly reduce the losses compared to the two level bridge as discussed in (Tenner and Hofmann; 2010).

Modeling and control of ZSI

One of the first dynamic model developed for the ZSI impedance-network-capacitor-voltage control has been proposed in (Gajanayake et al.; 2005). Model was derived by using the conventional state-space averaging technique. The authors observed that when the ZSI is supplied from a voltage source, the transfer functions from the shoot-through duty cycle to the capacitor voltage and equivalent dc-link voltage contains a right-half plane (RHP) zero. Later, the same authors (Gajanayake et al.; 2007) showed that the effect of the RHP zero will propagate to the control of the ac-side voltage of the converter and proposed a method to improve the transient response. Similar results are provided in (Loh, Vilathgamuwa, Gajanayake, Lim and Teo; 2007). The authors in (Liu et al.; 2007) also observed an RHP zero and studied the location of the system poles and zeros when parameters of the impedance network are altered. Later, an average model based on circuit averaging technique is presented in (Galigekere and Kazimierczuk; 2013), which verified the results obtained by using the state-space models. The presence of RHP zeros tends to destabilize the wide-bandwidth feedback loops, implying high-gain instability and imposing control limitations. In addition, Upadhyay et al. (2011) have demonstrated that the mismatch in the impedance network parameters may compromise the stability of the capacitor voltage control due to the additional resonances and their effect on the phase

behavior of the control-to-capacitor voltage transfer function.

The use of Z-source inverter in PV applications was demonstrated in (Huang et al.; 2006) and the control design in grid-connected applications is discussed e.g. in (Liu et al.; 2013), (Gajanayake et al.; 2009), and Li et al. (2010). In grid-connected applications, the capacitor voltage control is the recommended control scheme of the inverter instead of the equivalent dc-link voltage control. The drawbacks of a equivalent dc-link voltage control have been discussed in (Tang et al.; 2010) and Li et al. (2010). The equivalent dc-link waveform is a pulsed waveform due to shoot-through states and the equivalent dc-link voltage reference should be modified according to the shoot-through duty cycle, whereas the impedance network capacitor voltage reference can be kept constant. Moreover, in the capacitor voltage control, the equivalent dc-link voltage is automatically as low as possible and the inverter bridge switching losses are minimized.

1.4 Motivation of the thesis

Small-signal modeling of switched-mode power converters has been widely studied topic since 1980s Middlebrook and Cuk (1977) since it provides deterministic methods to evaluate the performance of the converter under different control modes (Middlebrook; 1988). In addition, by using the small-signal model the impedance characteristics of the converter can be derived, which provides a simple tool to analyze the operation of the converter as a part of an interconnected system. Small-signal based modeling also enables taking into account the dual nature (highly non-linear current-voltage characteristics) of the PVG in control design of the interfacing power electronic converters, which will improve the control system quality as discussed in (Suntio et al.; 2009) (Suntio et al.; 2010). It is claimed that the small-signal methods have increased the product quality of a dc-dc converters significantly. Thus it is quite natural that an increased interest towards the small-signal methods for ac-systems have been observed as the number of electric systems with power-converter-based sources and loads is constantly increasing.

Grid-connected inverters have been shown to increase the harmonic distortion in the grid (Enslin and Heskes; 2004) and may even compromise the system stability (Wan et al.; 2013). To analyze these interactions, an impedance-based stability-criteria have been proposed (Sun; 2011). The measured impedance provides tools to analyze the interactions, although the measurements may be difficult to be implement in practice. Thus the models that can predict the impedance characteristics are highly desirable. In this thesis, a model to predict the output impedance of a ZSI is also proposed.

The single and two-stage VSI-based photovoltaic inverter have been demonstrated to contain a RHP-zero in the output current control when the converter is fed from a source having characteristics of a current-source. The presence of the RHP-zero will destabilize the control system of the inverter when wide bandwidth current control is utilized. Fortunately a dc-link voltage control with a sufficient bandwidth depending on the size of the dc-link capacitor can stabilize the inverter control system (Messo et al.; 2014). Due to the similarities in the converter topologies, a same tradeoff will be present also in ZSI. Component

selection of the Z-source inverter impedance network have been discussed e.g. in (Liu et al.; 2007), (Rajakaruna and Jayawickrama; 2010), and (Liu, Ge, Abu-Rub and Peng; 2014). In this thesis, a requirement for the impedance network capacitor is discussed to guarantee the small-signal stability.

1.5 Scientific contribution

The scientific contribution of the thesis can be summarized as:

- It was shown that the voltage-fed small-signal model fails to predict the small-signal characteristics of a grid-connected Z-source inverter when it is supplied from a source having high impedance (e.g. photovoltaic generator operating at current region). A small-signal model that takes into account the effect of the non-ideal source was derived.
- Based on the derived small-signal model, a design rule for the minimum value of the impedance network capacitor to guarantee the stable operation of ZSI was formulated. This limitation is removed if a feedback control system regulating the input voltage of the ZSI is utilized.
- A model to evaluate the effect of the asymmetric impedance network to the behavior of the inverter is derived. The mismatch in the impedance network components will cause additional resonances in the impedance network and result undesired oscillations during the disturbances. However, these oscillations are negligible and not visible at the input and output terminals of the converter.
- Differences between the dynamic properties of ZSI and VSI (single and two-stage) are presented. It is concluded that the dynamic properties of photovoltaic ZSI is comparable to VSI-based two-stage PV inverter.

Related papers

The ideas presented in this thesis are partly presented in the following publications:

- [P1] Jokipii, J. and Suntio, T. 'Input voltage control of a three-phase Z-source inverter in photovoltaic applications', in *IEEE PEDG 2013, Rogers, AR, USA*. pp 1-8.
- [P2] Jokipii, J., Messo, T and Suntio, T. 'Simple method for measuring output impedance of a three-phase inverter in dq-domain', in *IEEE IPEC 2014, Hiroshima, Japan*, pp. 1466–1470.
- [P3] Jokipii, J. and Suntio, T. 'Dynamic characteristics of three-phase Z-source-based photovoltaic inverter with asymmetric impedance network', in *IEEE ICPE 2015, Seoul, South-Korea*, pp. 1976–1983.
- [P4] Messo, T., Jokipii, J., Puukko, J. and Suntio, T. 'Determining the value of DC-link capacitance to ensure stable operation of a three-phase photovoltaic inverter', in *IEEE Trans. Power Electron.*, vol. 29, no. 2, pp. 665-673, 2014.

- [P5] Messo, T., Jokipii, J., Mäkinen, A., and Suntio, T. 'Modeling the grid synchronization induced negative-resistor-like behavior in the output impedance of a three-phase photovoltaic inverter', in *IEEE PEDG 2013, Rogers, AR, USA*, pp. 1-7.

In [P1], [P2], and [P3] author carried out the presented analysis, designed and built the prototype converter, and conducted the laboratory measurements. Dr. Tech. Messo helped with the proofreading, implementing the required laboratory setup, and the actual laboratory measurements. Prof. Suntio as a supervisor of the conducted research provided valuable ideas and comments regarding the analysis and terminology related to small-signal modeling of power converters and writing publications. In [P4] and [P5], where the main author was Dr. Tech. Messo, the author designed and built part of the required laboratory setup and helped with proofreading the papers. The author also contributed to the analysis carried out in [P4] and [P5].

1.6 Structure of the thesis

Chapter 2 presents the background of the thesis by introducing a method to derive small-signal model for single and two-stage VSI-based PV inverter by combining model of a voltage-fed VSI and the source subsystems. In Chapter 3, the same voltage-fed VSI model is used to develop the model of a voltage-fed and current-fed ZSI. Chapter 4 presents model for a photovoltaic ZSI and discusses the control design issues related to the inverter. Chapter 5 provides comparison between the dynamic properties of the ZSI and the VSI-based PV inverters. Finally conclusions and recommended future topics are presented in Chapter 6.

2 DYNAMIC CHARACTERIZATION OF VOLTAGE-SOURCE INVERTERS

This chapter introduces the small-signal modeling method used in this thesis by presenting a model for a grid-connected three-phase voltage-source inverter (VSI), which will be further developed to represent the small-signal characteristics of a single and a two-stage VSI-based photovoltaic inverter and Z-source inverter (ZSI).

2.1 On small-signal modeling of interfacing power electronic converters

Interfacing power electronic converters transfer energy between two electrical system, the source and load. Often, these interfacing converters are classified only based on the voltage levels at the input and output terminals, phase number, or type of system (dc or ac) but the fundamental nature of the source and load subsystem is usually neglected. Neglecting the behavior of the source and load may be justified when the static steady-state operation of the converter is analyzed, e.g. when studying efficiency or pulse-width modulation methods, since they do not affect to the results. However, when the dynamic behavior of the converters are analyzed, the type of load and source will affect the results and must be thus taken into account. Each interfacing power converter inherits four conversion schemes that are dictated by the type of source, load, and control-mode (Suntio et al.; 2009), (Suntio et al.; 2014). These conversion schemes together with the corresponding two-port network models are introduced in Fig. 2.1.

In the state-space-averaging and circuit-averaging techniques, the non-linear nature of a switched-mode power converter is removed by linearizing the operation of the converter at a steady-state operation point (Middlebrook; 1988), (Krein et al.; 1989). However, in the ac-systems, the steady state is sinusoidal, which effectively prevents using these methods as such. To overcome this limitation, several different methods to analyze the power converters in ac systems have been proposed. These include harmonic linearization (Sun; 2009), dynamic phasor theory (Mattavelli et al.; 1999), complex transfer functions (Gataric and Garrigan; 1999) and (Harnefors; 2007), and synchronous-reference-frame-based modeling (Hiti and Boroyevich; 1996). In synchronous-reference-frame-based modeling (dq-domain modeling), the sinusoidal quantities at the fundamental operating frequency are represented by constants, which allows applying conventional state-space-averaging techniques. It is worth noting that a conventional phasor theory including concept of symmetric components applies only to linear circuits operating at steady state. Nevertheless, it has been proven to be suitable for utility-power-system

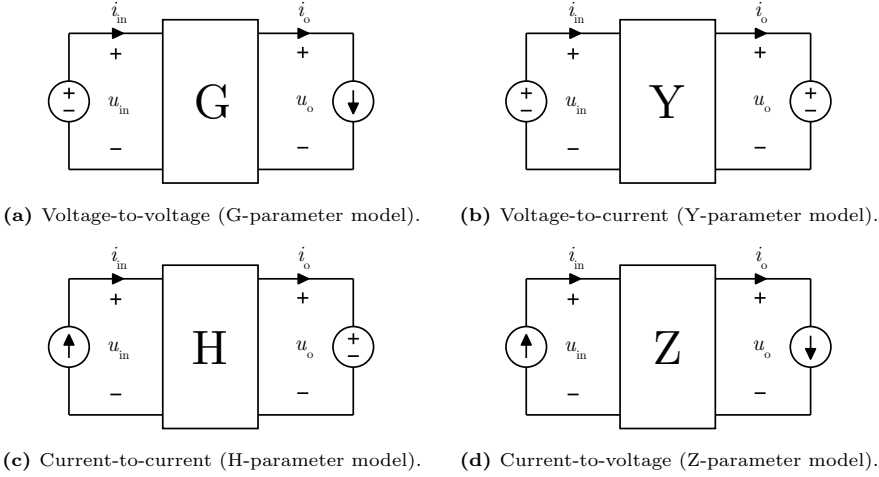


Figure 2.1. Four conversion schemes suitable for analyzing dynamic characteristics of interfacing power converters.

analysis for e.g. stability analysis of transmission lines and loads under the assumption that the amplitudes of voltages and currents change slowly with time such that their time derivatives can be assumed zero. The power converters, on the other hand, have high-bandwidth control loops and thus the conventional phasor theory is suitable only for steady-state analysis (Sun; 2009).

In grid-connected applications, the load of the power converter is the utility grid, which in an ideal case has a zero line impedance. In addition, in order to obtain high-quality currents, the power converters must be equipped with a high-bandwidth current control, hence the recommended conversion schemes to analyze dynamic behavior of a grid-connected power converter are the Y and H-parameter models (i.e. the voltage-to-current and current-to-current conversion schemes). Moreover, if the power converter is equipped with an input side voltage feedback control, as a photovoltaic inverter, it should be analyzed using the current-to-current conversion scheme (H-parameter model). Hence, the inverter interfacing the photovoltaic generators should be analyzed as a current-fed system. Unfortunately, this may cause misunderstanding as the inverters have been earlier classified as voltage-source and current-source inverter, based on the inverter power-stage-circuit structure instead of the type of the electrical energy source. The term voltage-source inverter (VSI) refers to the inverter bridge (switch matrix) topology, which requires that the dc-side voltage across the switch matrix retains its polarity and stays nearly constant during one switching period. Correspondingly, the current-source inverter (CSI) refers to the bridge, where the switch matrix dc-side current retains its polarity. To avoid misinterpretation, in this thesis, the term VSI is used to refer to the bridge topology, whereas term VSI-based inverter refers to a power converter, which contains the VSI-type inverter bridge and filter structures to comply with the requirements of the source and load.

Photovoltaic generator as an input source

As discussed in Chapter 1, the photovoltaic generator (PVG) is a highly non-linear source having properties of a current source and a voltage source. Its small-signal behavior have been demonstrated to behave as a simple RLC-circuit, whose parameters vary depending on the operation point. However, the impedance of the reactive components are relatively small compared to the impedance of the input capacitors typically used in power converters (Nousiainen et al.; 2013). Thus when the interconnected system of a photovoltaic generator and interfacing power converter is analyzed, the output impedance of the PVG can be approximated using its low-frequency value, i.e. the dynamic resistance ($r_{pv} = \hat{u}_{pv}/\hat{i}_{pv}$). The value of dynamic resistance varies from several ohms to several hundreds of ohms depending on the shape of the current-voltage curve and equals the static resistance ($R_{pv} = U_{pv}/I_{pv}$) at the maximum power point as illustrated in Fig. 2.2.

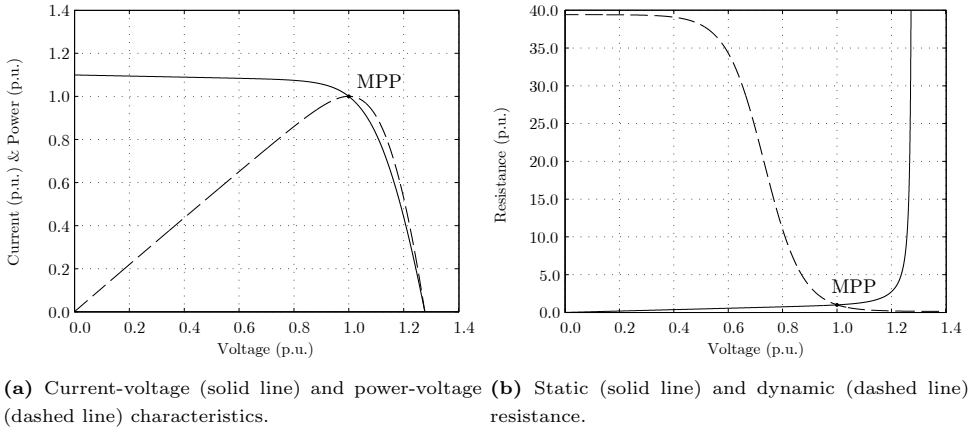


Figure 2.2. Electrical characteristics of a photovoltaic generator (PVG).

Three-phase VSI-based photovoltaic inverter

The power stage of a widely used three-phase inverter structure, a VSI-based inverter, is illustrated in Fig. 2.3 inside a dashed line. The inverter consists of an input capacitor (also known as the dc-link capacitor), VSI-type inverter bridge, and the grid-interfacing filter. In pulse-width-modulated power converter, the state of inverter bridge transistor is controlled by a pulse-width modulation & gate drive circuit, and operated by the control system of the inverter. The internal structure of the control system varies depending on the application (Blaabjerg et al.; 2006), however, it usually includes at least a high-bandwidth current control and grid synchronization.

In this thesis, the control scheme, which is illustrated in Fig. 2.4, is analyzed, in which the control objective is to set the operating point of the photovoltaic generator to its maximum power point. This is achieved by controlling the inverter dc-side capacitor voltage through a cascade connected feedback loops, where the fast current control forms the innermost control

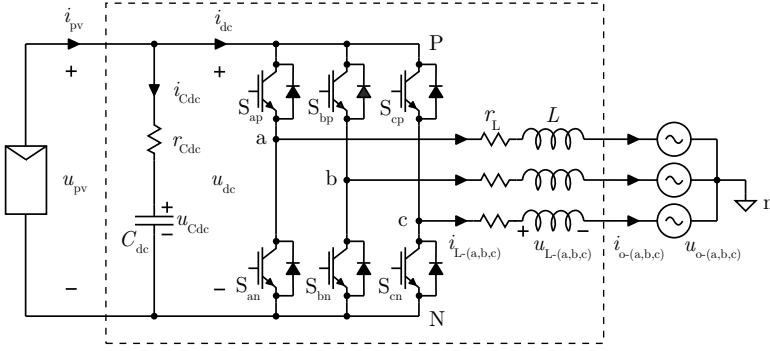


Figure 2.3. Three-phase grid-connected VSI-based photovoltaic inverter.

loop and slow voltage control loop the outer loop. In a space-vector-based current control, the direct and quadrature-component of the three-phase grid currents are controlled separately. In synchronous reference frame aligned according to the grid voltage space vector, the direct component current corresponds to the active power exchange and the quadrature component the reactive power exchange. As shown in Fig. 2.4, the capacitor voltage is controlled by adjusting the direct component of the current reference, i.e. the active power exchange. To align the control system reference frame correctly in respect to the grid synchronous reference frame, a phase-locked-loop is required. In the control system of Fig. 2.4, a conventional synchronous reference frame phase-locked-loop (SRF-PLL) is utilized.

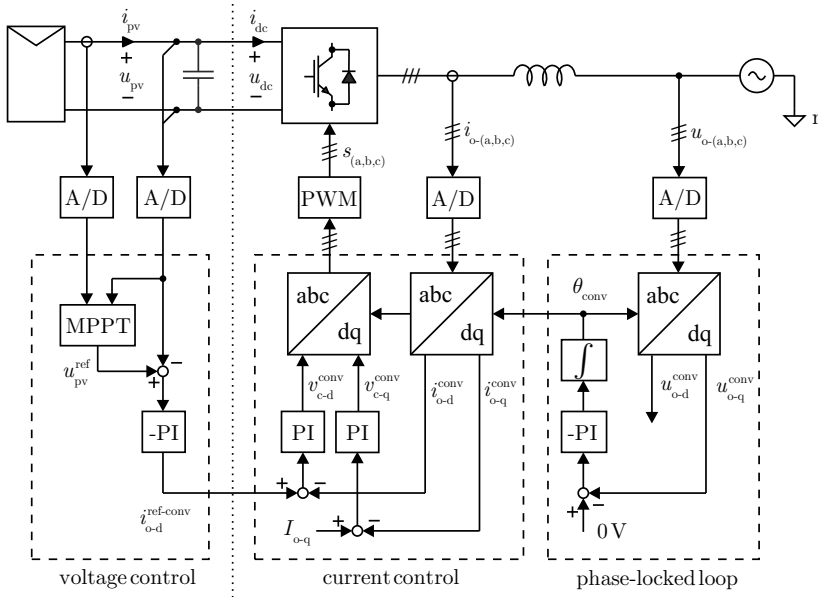


Figure 2.4. Overview of a cascade control scheme of the grid-connected inverter.

A detailed derivation of the small-signal model for a three-phase VSI-based inverter includ-

ing the current and voltage control is presented e.g. in (Puukko and Suntio; 2012). A method to include the effect of the PLL is presented in (Messo et al.; 2013). In this chapter, it is shown that the same H-parameter model of the VSI-based PV inverter can be constructed also by combining the Y-parameter model of the voltage-fed VSI-based inverter and Z-parameter model of the photovoltaic generator and input capacitor. As the inverter stage (right side of the dashed line in converter of Fig. 2.4) of the VSI-based and Z-source inverter are identical, this method allows using the same voltage-fed VSI model in analysis of the Z-source inverter. The presence of the maximum-power-point tracker will be neglected in the analysis due to its slow dynamics.

2.2 Voltage-fed VSI-based grid-connected inverter

The power stage of a conventional voltage-fed VSI-based inverter is illustrated in Fig. 2.5. According to control engineering principles, the control inputs of the system are the duty ratios of the inverter-bridge-phase legs $d_{(a,b,c)}$ and the disturbance inputs are the dc-side voltage u_{dc} and the three-phase grid voltage $u_{o-(a,b,c)}$. To derive the two port model, the inverter dc-side current i_{dc} and the grid current $i_{o-(a,b,c)}$ shall be selected as the system output variables.

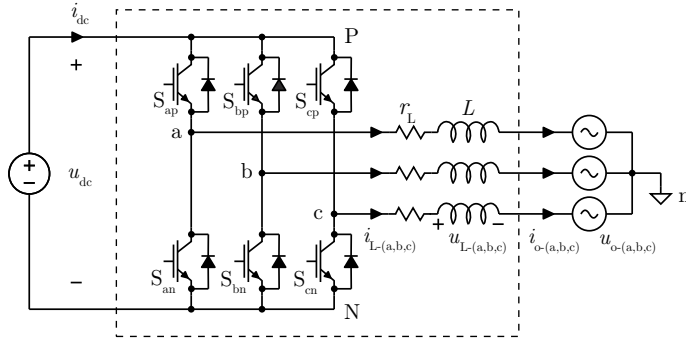


Figure 2.5. Voltage-fed three-phase VSI-based inverter.

2.2.1 Open-loop characteristics

Averaging the operation of the voltage-fed VSI-based inverter of Fig. 2.5 over one switching period yields

$$L \frac{d}{dt} \begin{bmatrix} \langle i_{L-a} \rangle \\ \langle i_{L-b} \rangle \\ \langle i_{L-c} \rangle \end{bmatrix} = \langle u_{dc} \rangle \begin{bmatrix} d_a \\ d_b \\ d_c \end{bmatrix} - (r_L + r_{sw}) \begin{bmatrix} \langle i_{L-a} \rangle \\ \langle i_{L-b} \rangle \\ \langle i_{L-c} \rangle \end{bmatrix} - \begin{bmatrix} \langle u_{o-a} \rangle \\ \langle u_{o-b} \rangle \\ \langle u_{o-c} \rangle \end{bmatrix} - \begin{bmatrix} \langle u_{nN} \rangle \\ \langle u_{nN} \rangle \\ \langle u_{nN} \rangle \end{bmatrix} \quad (2.1a)$$

and

$$\langle i_{dc} \rangle = d_a \langle i_{L-a} \rangle + d_b \langle i_{L-b} \rangle + d_c \langle i_{L-c} \rangle = \begin{bmatrix} \langle d_a \rangle \\ \langle d_b \rangle \\ \langle d_c \rangle \end{bmatrix}^T \cdot \begin{bmatrix} \langle i_{L-a} \rangle \\ \langle i_{L-b} \rangle \\ \langle i_{L-c} \rangle \end{bmatrix}, \quad (2.1b)$$

where $d_{(a,b,c)}$ are the duty ratios of each phase leg, r_{sw} is the on-state resistance of the transistor and its anti-parallel diode (assumed to be equal), and u_{nN} is the zero-sequence voltage produced by the inverter bridge. In (2.1), the angle brackets are used to represent the moving average of the corresponding quantity (averaged over one switching cycle).

The average model of the inverter, given in (2.1), may be written as an equivalent two-phase system in synchronous reference frame by applying the transformations presented explicitly in Appendix A. Zero sequence is neglected, since due to three-wire connection the zero sequence current cannot flow. The model in the synchronous reference frame can be given by

$$L \frac{d}{dt} \begin{bmatrix} \langle i_{L-d} \rangle \\ \langle i_{L-q} \rangle \end{bmatrix} = \begin{bmatrix} -(r_L + r_{sw}) & \omega_s L \\ -\omega_s L & -(r_L + r_{sw}) \end{bmatrix} \begin{bmatrix} \langle i_{L-d} \rangle \\ \langle i_{L-q} \rangle \end{bmatrix} + \langle u_{dc} \rangle \begin{bmatrix} d_d \\ d_q \end{bmatrix} - \begin{bmatrix} \langle u_{o-d} \rangle \\ \langle u_{o-q} \rangle \end{bmatrix} \quad (2.2a)$$

and

$$\langle i_{dc} \rangle = \frac{3}{2} \begin{bmatrix} d_d \\ d_q \end{bmatrix}^T \cdot \begin{bmatrix} \langle i_{L-d} \rangle \\ \langle i_{L-q} \rangle \end{bmatrix}. \quad (2.2b)$$

In synchronous reference frame, the steady-state operating point is represented by constant quantities enabling the use of conventional linearization methods. In grid-connected inverter, the steady-state values of the dc-side voltage, dc-side current, and grid voltage are usually known, which can be used to obtain the linearization point (steady state) values of the duty cycles and output current by setting the time-derivatives in (2.2) to zero. The steady state operating point can be solved by using the equations

$$D_d^2 + \frac{2\omega_s L I_{o-q} - U_{o-d}}{U_{dc}} D_d + \frac{(\omega_s^2 L^2 + R_{dc}^2) I_{o-q}^2 - \omega_s L U_{o-d} I_{o-q}}{U_{dc}^2} - \frac{2I_{in} R_{eq}}{3U_{dc}} = 0 \text{ V} \quad (2.3a)$$

$$I_{o-d} = \frac{D_d U_{dc} + \omega_s L I_{o-q} - U_{o-d}}{R_{eq}} \quad (2.3b)$$

$$D_q = \frac{\omega_s L I_{o-d} + R_{eq} I_{o-q}}{U_{dc}} \quad (2.3c)$$

$$R_{eq} = r_L + r_{sw}, \quad U_{o-q} = 0 \text{ V}, \quad I_{L-d} = I_{o-d}, \quad I_{L-q} = I_{o-q} = \frac{3}{2U_{o-d}} Q, \quad (2.3d)$$

where Q is the steady-state value of the reactive power drawn by the inverter (usually set to zero). In synchronous reference frame aligned to grid-voltage space vector, the steady-state value of the grid-voltage q-component is zero.

The average model of (2.2) can be linearized at the steady-state operating point given by (2.3) resulting a linearized state-space model of the inverter. The linearized model in Laplace

domain using conventional state-space representation can be given by

$$s \underbrace{\begin{bmatrix} \hat{i}_{L-d} \\ \hat{i}_{L-q} \end{bmatrix}}_{\mathbf{x}} = \underbrace{\begin{bmatrix} -\frac{r_L+r_{sw}}{L} & \omega_s \\ -\omega_s & -\frac{r_L+r_{sw}}{L} \end{bmatrix}}_{\mathbf{A}} \underbrace{\begin{bmatrix} \hat{i}_{L-d} \\ \hat{i}_{L-q} \end{bmatrix}}_{\mathbf{x}} + \underbrace{\begin{bmatrix} \frac{D_d}{L} & -\frac{1}{L} & 0 & \frac{U_{dc}}{L} & 0 \\ \frac{D_q}{L} & 0 & -\frac{1}{L} & 0 & \frac{U_{dc}}{L} \end{bmatrix}}_{\mathbf{B}} \underbrace{\begin{bmatrix} \hat{u}_{dc} \\ \hat{u}_{o-d} \\ \hat{u}_{o-q} \\ \hat{d}_d \\ \hat{d}_q \end{bmatrix}}_{\mathbf{u}} \quad (2.4a)$$

and

$$\underbrace{\begin{bmatrix} \hat{i}_{dc} \\ \hat{i}_{o-d} \\ \hat{i}_{o-q} \end{bmatrix}}_{\mathbf{y}} = \underbrace{\begin{bmatrix} \frac{3D_d}{2} & \frac{3D_q}{2} \\ 1 & 0 \\ 0 & 1 \end{bmatrix}}_{\mathbf{C}} \underbrace{\begin{bmatrix} \hat{i}_{L-d} \\ \hat{i}_{L-q} \end{bmatrix}}_{\mathbf{x}} + \underbrace{\begin{bmatrix} 0 & 0 & 0 & \frac{3I_{o-d}}{2} & \frac{3I_{o-q}}{2} \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix}}_{\mathbf{D}} \underbrace{\begin{bmatrix} \hat{u}_{dc} \\ \hat{u}_{o-d} \\ \hat{u}_{o-q} \\ \hat{d}_d \\ \hat{d}_q \end{bmatrix}}_{\mathbf{u}}, \quad (2.4b)$$

where \mathbf{x} presents the state variables, \mathbf{u} the input variables, and \mathbf{y} the output variables. Thus the inverter model can be formulated as

$$\begin{cases} s\mathbf{x} = \mathbf{Ax} + \mathbf{Bu} \\ \mathbf{y} = \mathbf{Cx} + \mathbf{Du}. \end{cases} \quad (2.5)$$

Transfer functions of the voltage-fed VSI-based inverter

The state space representation given in (2.5) provides a simple method to compute all the transfer functions of the inverter. The system output as a function of the input variables can be solved using (2.6). Due to the complexity of the system, matrix manipulation software such as MATLAB is required to perform the computation.

$$\mathbf{y} = [\mathbf{C}(s\mathbf{I} - \mathbf{A})^{-1}\mathbf{B} + \mathbf{D}]\mathbf{u} = \mathbf{Gu} \quad (2.6)$$

Since the system has five input variables and three output variables a total of fifteen transfer functions is obtained as shown in (2.7). These transfer functions are presented explicitly in Appendix B.

$$\underbrace{\begin{bmatrix} \hat{i}_{dc} \\ \hat{i}_{o-d} \\ \hat{i}_{o-q} \end{bmatrix}}_{\mathbf{y}} = \underbrace{\begin{bmatrix} Y_{in} & T_{oi-d} & T_{oi-q} & G_{ci-d} & G_{ci-q} \\ G_{io-d} & -Y_{o-d} & -Y_{o-qd} & G_{co-d} & G_{co-qd} \\ G_{io-q} & -Y_{o-dq} & -Y_{o-q} & G_{co-dq} & G_{co-q} \end{bmatrix}}_{\mathbf{G}} \underbrace{\begin{bmatrix} \hat{u}_{dc} \\ \hat{u}_{o-d} \\ \hat{u}_{o-q} \\ \hat{d}_d \\ \hat{d}_q \end{bmatrix}}_{\mathbf{u}} \quad (2.7)$$

Using the derived transfer functions, the input and the output dynamics of the converter can be given by

$$\hat{i}_{dc} = Y_{in}\hat{u}_{dc} + T_{oi-d}\hat{u}_{o-d} + T_{oi-q}\hat{u}_{o-q} + G_{ci-d}\hat{d}_d + G_{ci-q}\hat{d}_q \quad (2.8)$$

and

$$\begin{aligned} \hat{i}_{o-d} &= G_{io-d}\hat{u}_{dc} - Y_{o-d}\hat{u}_{o-d} - Y_{o-qd}\hat{u}_{o-q} + G_{co-d}\hat{d}_d + G_{co-qd}\hat{d}_q \\ \hat{i}_{o-q} &= G_{io-q}\hat{u}_{dc} - Y_{o-dq}\hat{u}_{o-d} - Y_{o-q}\hat{u}_{o-q} + G_{co-dq}\hat{d}_d + G_{co-q}\hat{d}_q, \end{aligned} \quad (2.9)$$

respectively. The output terminal of the model is divided into direct and quadrature components, i.e. the model has three terminals. Fortunately, the complexity of the model can be reduced by utilizing transfer matrices to represent the input and output dynamics

$$\hat{i}_{dc} = Y_{in}\hat{u}_{dc} + \underbrace{\begin{bmatrix} T_{oi-d} & T_{oi-q} \end{bmatrix}}_{\mathbf{T}_{oi}} \begin{bmatrix} \hat{u}_{o-d} \\ \hat{u}_{o-q} \end{bmatrix} + \underbrace{\begin{bmatrix} G_{ci-d} & G_{ci-q} \end{bmatrix}}_{\mathbf{G}_{ci}} \begin{bmatrix} \hat{d}_d \\ \hat{d}_q \end{bmatrix} \quad (2.10)$$

and

$$\begin{aligned} \begin{bmatrix} \hat{i}_{o-d} \\ \hat{i}_{o-q} \end{bmatrix} &= \underbrace{\begin{bmatrix} G_{io-d} \\ G_{io-q} \end{bmatrix}}_{\mathbf{G}_{io}} \hat{u}_{dc} - \underbrace{\begin{bmatrix} Y_{o-d} & Y_{o-qd} \\ Y_{o-dq} & Y_{o-q} \end{bmatrix}}_{\mathbf{Y}_o} \begin{bmatrix} \hat{u}_{o-d} \\ \hat{u}_{o-q} \end{bmatrix} \\ &\quad + \underbrace{\begin{bmatrix} G_{co-d} & G_{co-qd} \\ G_{co-dq} & G_{co-q} \end{bmatrix}}_{\mathbf{G}_{co}} \begin{bmatrix} \hat{d}_d \\ \hat{d}_q \end{bmatrix}. \end{aligned} \quad (2.11)$$

Furthermore, the use of transfer matrices can be utilized to obtain a linear two-port model (2.12), which can be visualized by an equivalent circuit shown in Fig. 2.6 or control-block diagram shown in Fig 2.7. The notations are the same that has been successfully used to analyze the dc-dc converters.

$$\begin{bmatrix} \hat{i}_{dc} \\ \hat{i}_o \end{bmatrix} = \begin{bmatrix} Y_{in} & \mathbf{T}_{oi} & \mathbf{G}_{ci} \\ \mathbf{G}_{io} & -\mathbf{Y}_o & \mathbf{G}_{co} \end{bmatrix} \begin{bmatrix} \hat{u}_{dc} \\ \hat{\mathbf{u}}_o \\ \hat{\mathbf{d}} \end{bmatrix} \quad (2.12)$$

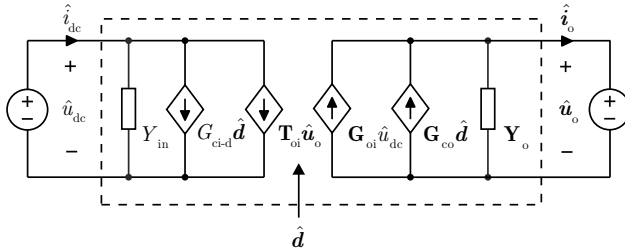


Figure 2.6. Linear two-port model of voltage-fed grid-connected inverter.

Phase-locked loop

The block-diagram of a conventional synchronous-reference-frame phase-locked loop (SRF-PLL) was illustrated previously in Fig. 2.4. The inputs of the PLL are the measured phase or line voltages and the output is the instantaneous electrical angle of the grid voltage space vector. For determining the instantaneous angle of the grid-voltage space vector, it is assumed that the quadrature component of the grid-voltage in SRF is zero.

Previously, the model of the inverter was derived in the synchronous-reference frame rotating at a constant frequency. The block-diagram of the conventional phase-locked loop represented in the same synchronous reference frame is shown in Fig. 2.8. At the steady state, the angles of the synchronous reference frame (θ_{grid}) and the control system reference frame (θ_{conv}) are equal. However, if a perturbation is added to the quadrature component of the grid voltage (e.g. due to unbalance or frequency deviation), the PLL will adjust the control-system-reference-frame electrical angle accordingly.

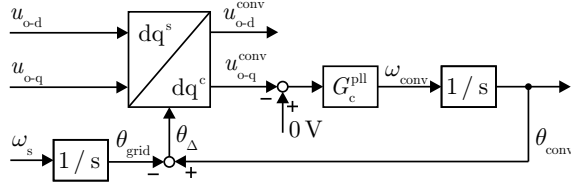


Figure 2.8. Synchronous reference frame phase-locked loop. Inputs in synchronous reference frame.

As discussed in (Messo et al.; 2013), the PLL small-signal model shown in Fig. 2.9, which is suitable for the control design of the PLL controller, can be obtained by linearizing the space-vector transformation mapping the quantities between the synchronous reference frame and control system reference frame. Transferring arbitrary quantity $x_{(d,q)}$ between the synchronous reference frame and control system reference frame (denoted by superscript conv) is defined as follows (see Appendix A):

$$x_d^{\text{conv}} = \cos \theta_{\Delta} x_d + \sin \theta_{\Delta} x_q \quad (2.16a)$$

and

$$x_q^{\text{conv}} = -\sin \theta_{\Delta} x_d + \cos \theta_{\Delta} x_q, \quad (2.16b)$$

where the angle difference between the synchronous reference frame and control system reference frame is $\theta_{\Delta} = \theta_{\text{conv}} - \theta_{\text{grid}}$. Linearizing (2.16) yields

$$\hat{x}_d^{\text{conv}} = \hat{x}_d + \hat{\theta}_{\Delta} X_q \quad (2.17a)$$

and

$$\hat{x}_q^{\text{conv}} = \hat{x}_q - \hat{\theta}_{\Delta} X_d. \quad (2.17b)$$

Based on (2.17), the transfer function from angle difference $\hat{\theta}_\Delta$ to the sensed q-component of the grid-voltage equals $-1/U_{o-d}$. The resulting loop gain of the system of Fig. 2.9 equals $L_{pll} = -U_{o-d}G_c^{pll}/s$. To regulate the sensed grid voltage q-component to zero, an inverting error amplifier G_c^{pll} is required to cancel the negative open-loop dc-gain.

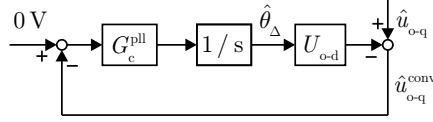


Figure 2.9. Small-signal model of SRF-PLL.

As the control scheme of the inverter is based on the current control in the converter reference frame, the small signal perturbation in the output voltage q-component will affect the current control through the sensed grid voltage electrical angle. According to Fig. 2.9, the angle difference can be given by

$$\hat{\theta}_\Delta = \frac{1}{U_{o-d}} \frac{L_{pll}}{1 + L_{pll}} \hat{u}_{o-q}, \quad (2.18)$$

where the PLL loop gain $L_{pll} = -U_{o-d}G_c^{pll}/s$.

The transformation required for representing the grid current in control system reference frame as a function of the synchronous reference frame quantities, based on (2.17) and (2.18), can be given as

$$\hat{\mathbf{i}}_o^{\text{conv}} = \mathbf{G}_{pll}^{\text{io}} \mathbf{G}_{se}^{\text{uo}} \hat{\mathbf{u}}_o + \mathbf{G}_{se}^{\text{io}} \hat{\mathbf{i}}_o, \quad (2.19)$$

where

$$\mathbf{G}_{pll}^{\text{io}} = \begin{bmatrix} 0 & \frac{I_{o-q}}{U_{o-d}} \frac{L_{pll}}{1 + L_{pll}} \\ 0 & -\frac{I_{o-d}}{U_{o-d}} \frac{L_{pll}}{1 + L_{pll}} \end{bmatrix} \quad (2.20)$$

Similarly, the required transformation for representing the PWM control signal in synchronous reference as a function of the control-system-reference-frame quantities can be given as

$$\hat{\mathbf{v}}_c = \mathbf{G}_{pll}^{\text{d}} \mathbf{G}_{se}^{\text{uo}} \hat{\mathbf{u}}_o + \hat{\mathbf{v}}_c^{\text{conv}}, \quad (2.21)$$

where

$$\mathbf{G}_{pll}^{\text{d}} = \begin{bmatrix} 0 & -\frac{D_q}{U_{o-d}} \frac{L_{pll}}{1 + L_{pll}} \\ 0 & \frac{D_d}{U_{o-d}} \frac{L_{pll}}{1 + L_{pll}} \end{bmatrix}. \quad (2.22)$$

Thus PLL-generates a feed-forward path from the output voltage to the output current.

Grid-current control

Under output current control scheme, illustrated in Fig. 2.4, the d and q-component of the inverter PWM control signal are adjusted by the current controller based on the difference between the current reference and the measured current, i.e.,

$$\hat{\mathbf{v}}_c^{\text{conv}} = \mathbf{G}_c^{\text{io}} \left(\hat{\mathbf{i}}_o^{\text{ref}} - \hat{\mathbf{i}}_o^{\text{conv}} \right), \quad (2.23)$$

where the current controller is

$$\mathbf{G}_c^{\text{io}} = \begin{bmatrix} G_c^{\text{io}} & 0 \\ 0 & G_c^{\text{io}} \end{bmatrix}. \quad (2.24)$$

Combining the effect of the PWM delay (2.14), phase-locked loop (2.21), and the current control (2.23), the synchronous reference frame duty ratio equals:

$$\hat{\mathbf{d}} = \mathbf{G}_{\text{pwm}} \left(\mathbf{G}_c^{\text{io}} \left(\hat{\mathbf{i}}_o^{\text{ref}} - \hat{\mathbf{i}}_o - \mathbf{G}_{\text{pll}}^{\text{io}} \hat{\mathbf{u}}_o \right) + \mathbf{G}_{\text{pll}}^{\text{d}} \hat{\mathbf{u}}_o \right). \quad (2.25)$$

To simplify the equations, and because the control system will be implemented in DSP, an unity sensing gain for the grid voltage and current is assumed in (2.25). A control-block diagram illustrating the current control scheme is depicted in Fig. 2.10. The block-diagram includes the sensing gain for the output voltage and output current.

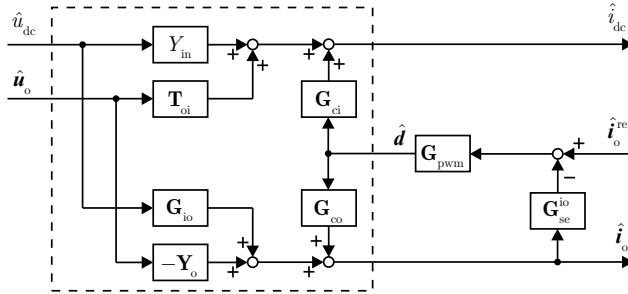


Figure 2.10. Control-block diagram of a synchronous reference frame output current control.

The transfer functions representing the dynamics of the output-current-controlled voltage-fed VSI can be used to obtain the two port model of the inverter shown in (2.26) as the linear equivalent circuit depicted in Fig. 2.11. Superscript 'out' is used to denote the transfer functions of an output-current-controlled converter. The system-control-input variable is now the output current reference.

$$\begin{bmatrix} \hat{i}_{\text{dc}} \\ \hat{\mathbf{i}}_o \end{bmatrix} = \begin{bmatrix} Y_{\text{in}}^{\text{out}} & \mathbf{T}_{\text{oi}}^{\text{out}} & \mathbf{G}_{\text{ri}}^{\text{out}} \\ \mathbf{G}_{\text{io}}^{\text{out}} & -\mathbf{Y}_o^{\text{out}} & \mathbf{G}_{\text{ro}}^{\text{out}} \end{bmatrix} \begin{bmatrix} \hat{u}_{\text{dc}} \\ \hat{\mathbf{u}}_o \\ \hat{\mathbf{i}}_o^{\text{ref}} \end{bmatrix} \quad (2.26)$$

The closed-loop transfer functions of the output-current-controlled voltage-fed VSI-based inverter, given in (2.26), can be obtained by inserting the duty ratio given in (2.25) to the transfer functions representing the open-loop dynamics (2.12), or alternatively from Fig. 2.10. The closed loop dynamics can be given as follows

$$Y_{\text{in}}^{\text{out}} = Y_{\text{in}} - \mathbf{G}_{\text{ci}} \mathbf{G}_{\text{pwm}} \mathbf{G}_c^{\text{io}} \mathbf{S}^{\text{out}} \mathbf{G}_{\text{io}} \quad (2.27a)$$

$$\mathbf{T}_{\text{oi}}^{\text{out}} = \mathbf{T}_{\text{oi}} + \mathbf{G}_{\text{ci}} \mathbf{G}_{\text{pwm}} \mathbf{G}_{\text{pll}}^{\text{d}} + \mathbf{G}_{\text{ci}} \mathbf{G}_{\text{pwm}} \mathbf{G}_c^{\text{io}} \mathbf{S}^{\text{out}} \left(\mathbf{Y}_o - \mathbf{G}_{\text{pll}}^{\text{io}} - \mathbf{G}_{\text{co}} \mathbf{G}_{\text{pwm}} \mathbf{G}_{\text{pll}}^{\text{d}} \right) \quad (2.27b)$$

$$\mathbf{G}_{\text{ri}}^{\text{out}} = \mathbf{G}_{\text{ci}} \mathbf{G}_{\text{pwm}} \mathbf{G}_c^{\text{io}} \mathbf{S}^{\text{out}} \quad (2.27c)$$

$$\mathbf{G}_{io}^{\text{out}} = \mathbf{S}^{\text{out}} \mathbf{G}_{io} \quad (2.27d)$$

$$\mathbf{Y}_o^{\text{out}} = \mathbf{S}^{\text{out}} \mathbf{Y}_o + \mathbf{T}_{\text{out}} \mathbf{G}_{\text{pll}}^{\text{io}} - \mathbf{S}^{\text{out}} \mathbf{G}_{\text{co}} \mathbf{G}_{\text{pwm}} \mathbf{G}_{\text{pll}}^{\text{d}} \quad (2.27e)$$

$$\mathbf{G}_{ro}^{\text{out}} = \mathbf{T}^{\text{out}} \quad (2.27f)$$

where the sensitivity function can be given by

$$\mathbf{S}^{\text{out}} = (\mathbf{I} + \mathbf{G}_{\text{co}} \mathbf{G}_{\text{pwm}} \mathbf{G}_{\text{c}}^{\text{io}})^{-1} \quad (2.28)$$

and the input-to-output transfer matrix by

$$\mathbf{T}^{\text{out}} = \mathbf{G}_{\text{co}} \mathbf{G}_{\text{pwm}} \mathbf{G}_{\text{c}}^{\text{io}} (\mathbf{I} + \mathbf{G}_{\text{co}} \mathbf{G}_{\text{pwm}} \mathbf{G}_{\text{c}}^{\text{io}})^{-1}. \quad (2.29)$$

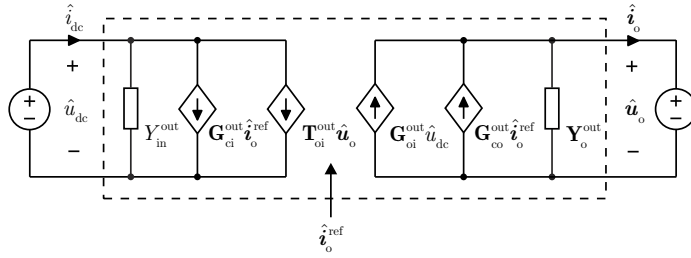


Figure 2.11. Linear model of VSI supplied from an ideal voltage source.

2.2.3 The effect of non-ideal source on dynamics of VSI-based inverter

Most often, the input source of the VSI-based inverter is not an ideal voltage source but as e.g. in photovoltaic applications the source is the photovoltaic generator and a large capacitor is connected at the input terminal. In addition, the photovoltaic inverter is equipped with the dc-side voltage control, which must be included also in the model. As the photovoltaic inverter is an input-voltage-regulated, the source cannot be modeled as an ideal voltage source having zero internal impedance. The interconnection of a voltage-fed VSI-based inverter and an arbitrary current-fed source subsystem is illustrated in Fig. 2.12. In a VSI-based inverter, where the source impedance is non-zero, the dc-side voltage \hat{u}_{dc} of the inverter bridge is not an independent input variable, instead it depends on the current drawn by the inverter \hat{i}_{dc} . The two-port model determining the transfers function between the dc-side current \hat{i}_{dc} and and dc-side \hat{u}_{dc} , i.e. two port model of the source subsystem, can be given as:

$$\begin{bmatrix} \hat{u}_{\text{in}} \\ \hat{u}_{\text{dc}} \end{bmatrix} = \begin{bmatrix} Z_{\text{in}} & T_{\text{oi}} \\ G_{\text{io}} & -Z_{\text{o}} \end{bmatrix} \begin{bmatrix} \hat{i}_{\text{in}} \\ \hat{i}_{\text{dc}} \end{bmatrix}. \quad (2.30)$$

To include the effect of the non-ideal source into the dynamics of the inverter, the two-port models of the inverter given in (2.12) and the source subsystem given in (2.30) are combined.

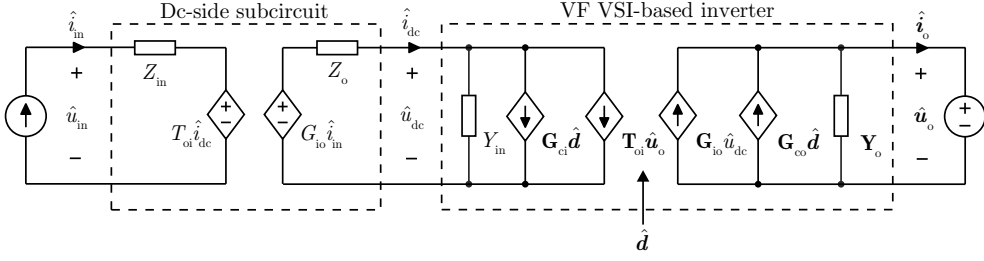


Figure 2.12. Linear model of the output current-controlled VSI supplied from a non-ideal source.

The two-port model characterizing the interconnected system, i.e. the source-affected VSI-based inverter, can be given by

$$\begin{bmatrix} \hat{u}_{in} \\ \hat{i}_o \end{bmatrix} = \begin{bmatrix} Z_{in}^S & \mathbf{T}_{oi}^S & \mathbf{G}_{ci}^S \\ \mathbf{G}_{io}^S & -\mathbf{Y}_o^S & \mathbf{G}_{co}^S \end{bmatrix} \begin{bmatrix} \hat{i}_{in} \\ \hat{u}_o \\ \hat{d} \end{bmatrix} \quad (2.31)$$

where the superscript 'S' refers to the transfer functions including the effect of the non-ideal source. The transfer functions including the source-effect in (2.31) can be given by

$$Z_{in}^S = Z_{in}^{dc} + T_{oi}^{dc} \frac{Y_{in}^{vsi} G_{io}^{dc}}{1 + Z_o^{dc} Y_{in}^{vsi}} \quad (2.32a)$$

$$\mathbf{T}_{oi}^S = T_{oi}^{dc} \frac{1}{1 + Y_{in}^{vsi} Z_o^{dc}} \mathbf{T}_{oi}^{vsi} \quad (2.32b)$$

$$\mathbf{G}_{ci}^S = T_{oi}^{dc} \frac{1}{1 + Y_{in}^{vsi} Z_o^{dc}} \mathbf{G}_{ci}^{vsi} \quad (2.32c)$$

$$\mathbf{G}_{io}^S = \mathbf{G}_{io}^{vsi} \frac{G_{io}^{dc}}{1 + Z_o^{dc} Y_{in}^{vsi}} \quad (2.32d)$$

$$\mathbf{Y}_o^S = \mathbf{Y}_o^{vsi} + \mathbf{G}_{io}^{vsi} \frac{Z_o^{dc}}{1 + Z_o^{dc} Y_{in}^{vsi}} \mathbf{T}_{oi}^{vsi} \quad (2.32e)$$

$$\mathbf{G}_{co}^S = \mathbf{G}_{co}^{vsi} - \mathbf{G}_{io}^{vsi} \frac{Z_o^{dc}}{1 + Z_o^{dc} Y_{in}^{vsi}} \mathbf{G}_{ci}^{vsi}, \quad (2.32f)$$

where superscript 'dc' and 'vsi' are used to denote the transfer functions of the source sub-system and the VSI, respectively.

Moreover, in the interconnected system the dc-link voltage is no longer the input variable of the system. As a consequence, the new system input variables can be used to regulate the dc-link voltage, i.e. the dc-link voltage can be taken as a feedback variable. The dynamics associated to the dc-link voltage can be given by

$$\begin{bmatrix} \hat{u}_{dc} \end{bmatrix} = \begin{bmatrix} \mathbf{G}_{idc}^S & \mathbf{G}_{odc}^S & \mathbf{G}_{cdc}^S \end{bmatrix} \begin{bmatrix} \hat{i}_{ph} & \hat{u}_o & \hat{d} \end{bmatrix}^T, \quad (2.33)$$

where

$$\mathbf{G}_{idc}^S = \frac{1}{1 + Z_o^{dc} Y_{in}^{vsi}} G_{io}^{dc} \quad (2.34a)$$

$$G_{\text{odc}}^S = -\frac{Z_o^{\text{dc}}}{1 + Z_o^{\text{dc}} Y_{\text{in}}^{\text{vsi}}} \mathbf{T}_{\text{oi}}^{\text{vsi}} \quad (2.34b)$$

$$G_{\text{cdc}}^S = -\frac{Z_o^{\text{dc}}}{1 + Z_o^{\text{dc}} Y_{\text{in}}^{\text{vsi}}} G_{\text{ci}}^{\text{vsi}} \quad (2.34c)$$

The equations presented above to compute the source-affected transfer functions are valid for an inverter operating at open loop and under output-current control, i.e. for models given in (2.12) and (2.26), respectively.

2.3 VSI-based single and two-stage photovoltaic inverters

It should be noted that the following modeling method for the photovoltaic VSI is not the most convenient to represent its dynamics (Puukko and Suntio; 2012). However, it provides a tool to compare the characteristics of the Z-source inverter and the VSI-based inverter, as a part of the power stage is the same in both of the converters.

2.3.1 Single-stage VSI-based photovoltaic inverter

The single-stage photovoltaic inverter is supplied from a parallel connection of a photovoltaic generator and the input capacitor (also known as the dc-link capacitor). The source subsystem that will take into an account the effect of the capacitor and the photovoltaic generator according to Fig. 2.13 can be represented as:

$$\begin{bmatrix} \hat{u}_{\text{pv}} \\ \hat{u}_{\text{dc}} \end{bmatrix} = \begin{bmatrix} Z_{\text{eq}} & -Z_{\text{eq}} \\ Z_{\text{eq}} & -Z_{\text{eq}} \end{bmatrix} \begin{bmatrix} \hat{i}_{\text{ph}} \\ \hat{i}_{\text{dc}} \end{bmatrix}, \quad (2.35)$$

where

$$Z_{\text{eq}} = \frac{1}{Y_{\text{pv}} + Y_{\text{Cdc}}} = r_{\text{pv}} || Z_{\text{Cdc}} = \frac{r_{\text{pv}} \left(\frac{1}{sC_{\text{dc}}} + r_{\text{Cdc}} \right)}{r_{\text{pv}} + \frac{1}{sC_{\text{dc}}} + r_{\text{Cdc}}} = \frac{r_{\text{pv}} (1 + sC_{\text{dc}} r_{\text{Cdc}})}{sC_{\text{dc}} (r_{\text{pv}} + r_{\text{Cdc}}) + 1}. \quad (2.36)$$

The effect of the source subsystem can be included using the source affected model given in (2.31). However, since the current control is always required in VSI-based inverter, the source effect can be included directly to the output-current controlled inverter.

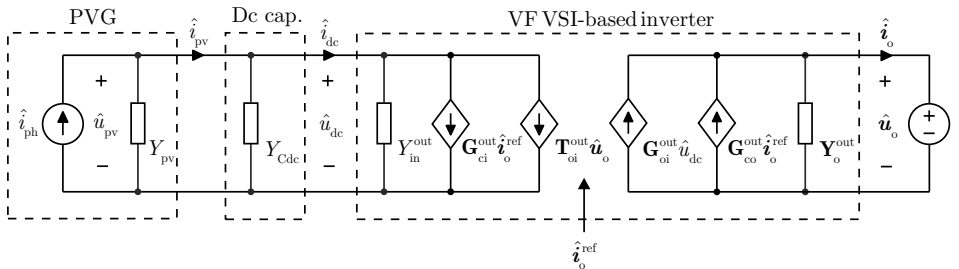


Figure 2.13. Linear model of the output current-controlled VSI supplied from a photovoltaic generator.

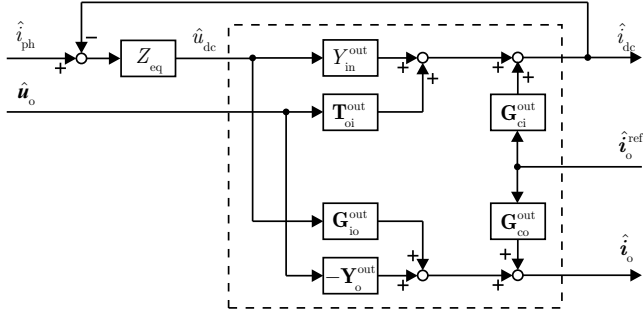


Figure 2.14. Including the effect of non-ideal source on current-controlled VSI-based inverter model. Dashed area represent the dynamics of the output-current-controlled inverter (see Fig. 2.10). An internal feedback loop is formed, where the loop gain equals $Z_{eq} Y_{in}^{out}$.

The two-port model characterizing the source-affected current-controlled VSI-based inverter can be given by

$$\begin{bmatrix} \hat{u}_{dc} \\ \hat{i}_o \end{bmatrix} = \begin{bmatrix} Y_{in}^{outS} & T_{oi}^{outS} & G_{ri}^{outS} \\ G_{io}^{outS} & -Y_o^{outS} & G_{ro}^{outS} \end{bmatrix} \begin{bmatrix} \hat{i}_{ph} \\ \hat{u}_o \\ \hat{i}_o^{ref} \end{bmatrix} \quad (2.37)$$

where the matrix elements are given explicitly in (2.38a) - (2.38f) and the superscript 'outS' refers to the output-current-controlled transfer functions including the effect of the non-ideal source.

$$Z_{in}^{outS} = \frac{Z_{eq}}{1 + Z_{eq} Y_{in}^{vsi-out}} \quad (2.38a)$$

$$T_{oi}^{outS} = -\frac{Z_{eq}}{1 + Z_{eq} Y_{in}^{vsi-out}} T_{oi}^{vsi-out} \quad (2.38b)$$

$$G_{ri}^{outS} = -\frac{Z_{eq}}{1 + Z_{eq} Y_{in}^{vsi-out}} G_{ri}^{vsi-out} \quad (2.38c)$$

$$G_{io}^{outS} = \frac{Z_{eq}}{1 + Z_{eq} Y_{in}^{vsi-out}} G_{io}^{vsi-out} \quad (2.38d)$$

$$Y_o^{outS} = Y_o^{vsi-out} + \frac{Z_{eq}}{1 + Z_{eq} Y_{in}^{vsi-out}} G_{io}^{vsi-out} T_{oi}^{vsi-out} \quad (2.38e)$$

$$G_{ro}^{outS} = G_{ro}^{vsi-out} - \frac{Z_{eq}}{1 + Z_{eq} Y_{in}^{vsi-out}} G_{io}^{vsi-out} G_{ri}^{vsi-out} \quad (2.38f)$$

The model given in (2.37) includes the effect of the non-ideal source and the current control. To include the input voltage control, the model of the output current controlled voltage-fed VSI-based inverter given in (2.26) is repeated in (2.39), with the exception that the small-signal value of the quadrature component of the output current reference is set to zero, since

according to Fig. 2.4, it is not affected by the dc-link-voltage controller. The model of the output-current controlled converter can be thus given by

$$\begin{bmatrix} \hat{u}_{dc} \\ \hat{i}_o \end{bmatrix} = \begin{bmatrix} Y_{in}^{outS} & T_{oi}^{outS} & G_{ri-d}^{outS} \\ G_{io}^{outS} & -Y_o^{outS} & G_{ro-d}^{outS} \end{bmatrix} \begin{bmatrix} \hat{i}_{ph} \\ \hat{u}_o \\ \hat{i}_{o-d}^{ref} \end{bmatrix} \quad (2.39)$$

where the control-to-output transfer function matrix equals

$$G_{ro-d}^{outS} = \begin{bmatrix} G_{ro-d}^{out} & G_{ro-dq}^{out} \end{bmatrix}^T. \quad (2.40)$$

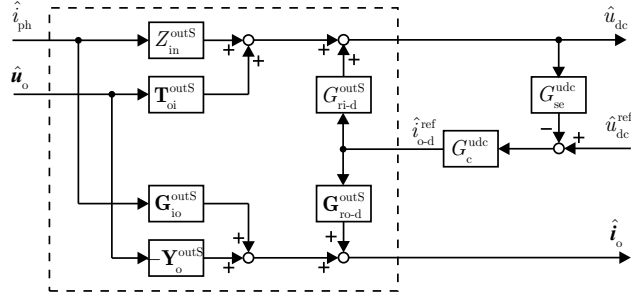


Figure 2.15. Control-block diagram of a dc-link voltage control.

The model is then used to include the effect of the dc-link-voltage control. Under the dc-link-voltage control, the converter direct-channel-current reference is given by the voltage controller according to

$$\hat{i}_{o-d}^{ref} = G_c^{udc} \left(\hat{u}_{dc}^{ref} - \hat{u}_{dc} \right), \quad (2.41)$$

where G_c^{udc} is the dc-link-voltage controller transfer function. Unity measurement gain is assumed.

Finally, the closed-loop transfer function including the effect of the dc-link-voltage control is found by substituting the current reference in (2.39) by the the output of the dc-link-voltage controller given in (2.41). The resulting closed-loop transfer functions of the system can be given by

$$\begin{bmatrix} \hat{u}_{dc} \\ \hat{i}_o \end{bmatrix} = \begin{bmatrix} Y_{in}^{inoutS} & T_{oi}^{inoutS} & G_{ri}^{inoutS} \\ G_{io}^{inoutS} & -Y_o^{inoutS} & G_{ro}^{inoutS} \end{bmatrix} \begin{bmatrix} \hat{i}_{ph} \\ \hat{u}_o \\ \hat{u}_{dc}^{ref} \end{bmatrix}, \quad (2.42)$$

where

$$Z_{in}^{inoutS} = \frac{1}{1 + G_{ri-d}^{outS} G_c^{udc}} Z_{in}^{outS} \quad (2.43a)$$

$$T_{oi}^{inoutS} = \frac{1}{1 + G_{ri-d}^{outS} G_c^{udc}} T_{oi}^{outS} \quad (2.43b)$$

$$G_{ri}^{inoutS} = \frac{G_{ri-d}^{outS} G_c^{udc}}{1 + G_{ri-d}^{outS} G_c^{udc}} \quad (2.43c)$$

$$\mathbf{G}_{io}^{inoutS} = \mathbf{G}_{io}^{outS} - \mathbf{G}_{ro-d}^{outS} G_c^{udc} \frac{1}{1 + G_{ri-d}^{outS} G_c^{udc}} \mathbf{Z}_{in}^{outS} \quad (2.43d)$$

$$\mathbf{Y}_o^{inoutS} = \mathbf{Y}_o^{outS} + \mathbf{G}_{ro-d}^{outS} G_c^{udc} \frac{1}{1 + G_{ri-d}^{outS} G_c^{udc}} \mathbf{T}_{oi}^{outS} \quad (2.43e)$$

$$\mathbf{G}_{ro}^{inoutS} = \mathbf{G}_{ro-d}^{outS} G_c^{udc} \frac{1}{1 + G_{ri-d}^{outS} G_c^{udc}}. \quad (2.43f)$$

The model given in (4.17) can be used to compute all the transfer functions of the VSI-based inverter operating at closed loop. The model produces the same results as the models that has been previously published e.g. in (Puukko and Suntio; 2012) and (Messo et al.; 2015) but it is formulated slightly differently.

2.3.2 Two-stage VSI-based photovoltaic inverter

The method to derive transfer functions of the two-stage VSI-based inverter is basically the same as in case of VSI-based inverter. The inverter dc-side subsystem is now the boost-stage fed by the photovoltaic generator. The circuit structure using the two-port models is shown in Fig. 2.16. When the boost-stage is operated at open loop, the control variable in Fig. 2.16 is the duty ratio of the boost-stage. In closed-loop operation, the control variable is the input voltage reference. The effect of the source subsystem to the inverter dynamics is now dictated by the output impedance of the voltage-boosting dc-dc stage and the dc-link capacitor.

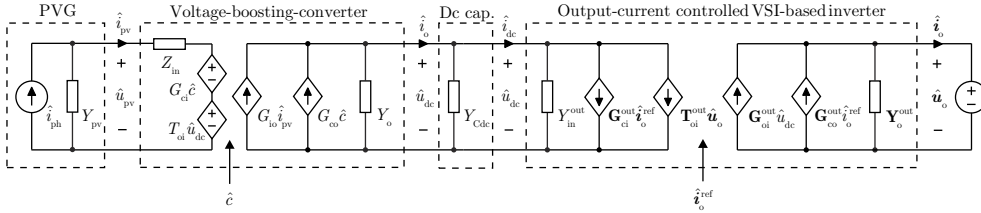


Figure 2.16. Linear model of the output current-controlled VSI supplied from a voltage-boosting dc-dc converter.

The effect of the nonzero source impedance on inverter dynamics can be included in the model by combining the H-parameter model of the voltage-boosting converter, the impedance of the dc-link capacitor, and the Y-parameter model of the VSI as illustrated in Fig. 2.16. The two-port model of the interconnected system can be given by

$$\begin{bmatrix} \hat{u}_{pv} \\ \hat{i}_o \end{bmatrix} = \begin{bmatrix} \mathbf{Z}_{in}^{outS} & \mathbf{T}_{oi}^{outS} & \mathbf{G}_{ri}^{outS} & \mathbf{G}_{ci}^{outS} \\ \mathbf{G}_{io}^{outS} & -\mathbf{Y}_o^{outS} & \mathbf{G}_{ro}^{outS} & \mathbf{G}_{co}^{outS} \end{bmatrix} \begin{bmatrix} \hat{i}_{ph} \\ \hat{u}_o \\ \hat{i}_o^{ref} \\ \hat{c} \end{bmatrix}, \quad (2.44)$$

where

$$\mathbf{Z}_{in}^{outS} = \mathbf{Z}_{in}^S + \frac{\mathbf{Z}_{eq}}{1 + \mathbf{Z}_{eq} \mathbf{Y}_{vsi-out}^S} \mathbf{G}_{io}^S \mathbf{T}_{oi}^S \quad (2.45a)$$

$$T_{oi}^{\text{outS}} = -T_{oi}^S \frac{Z_{eq}}{1 + Z_{eq}Y_{in}^{\text{vsi-out}}} \mathbf{T}_{oi}^{\text{vsi-out}} \quad (2.45b)$$

$$G_{ri}^{\text{outS}} = -T_{oi}^S \frac{Z_{eq}}{1 + Z_{eq}Y_{in}^{\text{vsi-out}}} \mathbf{G}_{ci}^{\text{vsi-out}} \quad (2.45c)$$

$$G_{ci}^{\text{outS}} = G_{ci}^S - T_{oi}^S \frac{Z_{eq}}{1 + Z_{eq}Y_{in}^{\text{vsi-out}}} G_{co}^S \quad (2.45d)$$

$$G_{io}^{\text{outS}} = \frac{Z_{eq}}{1 + Z_{eq}Y_{in}^{\text{vsi-out}}} G_{io}^S \mathbf{G}_{io}^{\text{vsi-out}} \quad (2.45e)$$

$$Y_o^{\text{outS}} = \mathbf{Y}_o^{\text{vsi-out}} + \frac{Z_{eq}}{1 + Z_{eq}Y_{in}^{\text{vsi-out}}} \mathbf{G}_{io}^{\text{vsi-out}} \mathbf{T}_{oi}^{\text{vsi-out}} \quad (2.45f)$$

$$G_{ro}^{\text{outS}} = \mathbf{G}_{co}^{\text{vsi-out}} - \frac{Z_{eq}}{1 + Z_{eq}Y_{in}^{\text{vsi-out}}} \mathbf{G}_{io}^{\text{vsi-out}} \mathbf{G}_{ci}^{\text{vsi-out}} \quad (2.45g)$$

$$G_{co}^{\text{outS}} = \frac{Z_{eq}}{1 + Z_{eq}Y_{in}^{\text{vsi-out}}} G_{co}^S \mathbf{G}_{io}^{\text{vsi-out}} \quad (2.45h)$$

Usually, as in single-stage inverter, the dc-link voltage is taken as a feedback variable. The dynamics of the dc-link voltage can be given by

$$\begin{bmatrix} \hat{u}_{dc} \end{bmatrix} = \begin{bmatrix} G_{idc}^{\text{outS}} & G_{odc}^{\text{outS}} & G_{rdc}^{\text{outS}} & G_{cdc}^{\text{outS}} \end{bmatrix} \begin{bmatrix} \hat{i}_{ph} & \hat{u}_o & \hat{i}_o^{\text{ref}} & \hat{c} \end{bmatrix}^T, \quad (2.46)$$

where

$$G_{idc}^{\text{outS}} = \frac{Z_{eq}}{1 + Z_{eq}Y_{in}^{\text{vsi-out}}} G_{io}^S \quad (2.47a)$$

$$G_{odc}^{\text{outS}} = -\frac{Z_{eq}}{1 + Z_{eq}Y_{in}^{\text{vsi-out}}} \mathbf{T}_{oi}^{\text{vsi-out}} \quad (2.47b)$$

$$G_{rdc}^{\text{outS}} = -\frac{Z_{eq}}{1 + Z_{eq}Y_{in}^{\text{vsi-out}}} \mathbf{G}_{ci}^{\text{vsi-out}} \quad (2.47c)$$

$$G_{cdc}^{\text{outS}} = \frac{Z_{eq}}{1 + Z_{eq}Y_{in}^{\text{vsi-out}}} G_{co}^S. \quad (2.47d)$$

In (2.45a) - (2.47d), the superscript 'S' denotes the source-affected transfer functions of the boost-stage, superscript 'vsi-out' the output-current-controlled VSI, and the equivalent source impedance equals

$$Z_{eq} = \frac{1}{Y_o^S + Y_{Cdc}}, \quad (2.48)$$

where Y_o^S is the output admittance of the boost-stage. The dc-link-voltage controller can then be included in the model using the same procedure as in the single-stage VSI-based inverter presented in Section 2.3.1.

2.4 Conclusions

This chapters proposed a method to characterize dynamics of a three-phase grid-connected single and two-stage VSI-based inverters utilizing the model of a conventional voltage-source-inverter. The models allow studying the operation of the inverter at open and closed loop including the conventional synchronous-reference-frame current control. The advantage of the presented modeling method is that the same voltage-fed VSI-based inverter model can be used in analysis of single-stage PV inverter, two stage PV inverter, and Z-source inverter as will be shown later.

3 DYNAMIC CHARACTERIZATION OF Z-SOURCE INVERTERS

This chapter presents the small signal models suitable for analyzing the open-loop characteristics of a three-phase voltage-fed and current-fed Z-source inverters (ZSI) in grid-connected applications. In addition, a comparison between the results obtained from the voltage-fed and the current-fed inverter are provided to justify the need of selecting correct two-port model in the analysis.

3.1 Modeling of a voltage-fed and current-fed Z-source inverters

A voltage-fed three-phase grid-connected Z-source inverter is illustrated in Fig. 3.1. The analysis of the ZSI can be carried out by using conventional averaging and linearization techniques in synchronous reference frame. However, since the converter has very large number of memory elements, the resulting transfer functions are very high order, which are tedious or even impossible to analyze as such. As a consequence, the model for a voltage-fed and current-fed ZSI is constructed by dividing the inverter into two subsystems, the impedance network and the VSI-based inverter.

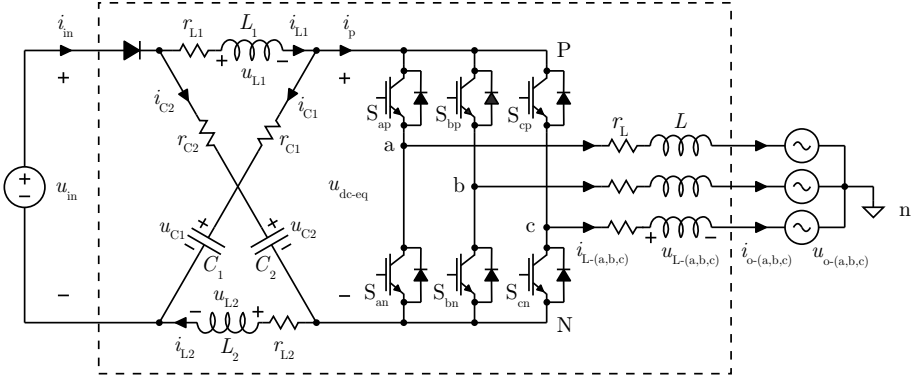


Figure 3.1. Voltage-fed three-phase Z-source inverter.

As discussed e.g. in (Gajanayake et al.; 2007) and (Li et al.; 2013), the impedance network and the inverter stage can be analyzed as two separate subsystems, where the shoot-through states are generated by an imaginary switch as shown in Fig. 3.2. As shown in Figs. 3.1 and 3.2, the impedance network and the VSI-based inverter parts are interconnected through the

equivalent dc-link. The current i_{dc} represent the current drawn by the inverter stage and the voltage u_{dc-eq} represents the equivalent dc-link voltage seen by inverter stage. The dc-side subsystem of the Z-source inverter is a voltage-fed impedance network. The output voltage of the impedance network is dictated by the sum of impedance network capacitor voltages and the input voltage, i.e. the output terminal is a voltage-type, and thus the voltage-fed impedance network must be analyzed using the voltage-to-voltage conversion scheme. Similar analysis is valid for a current-fed impedance network, which has to be analyzed as a current-to-voltage conversion scheme as will be shown later.

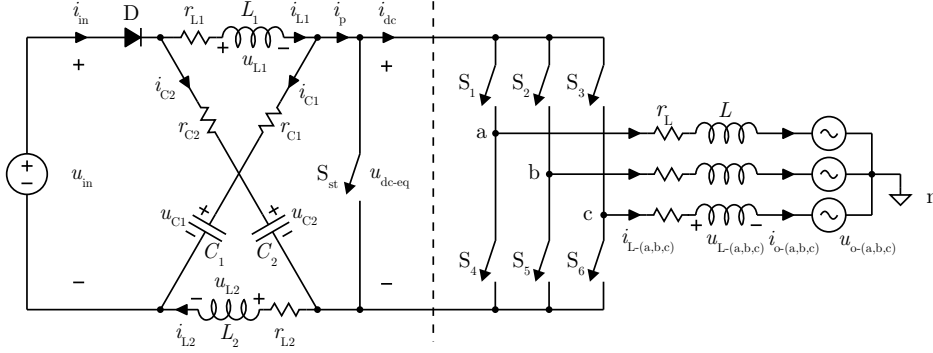


Figure 3.2. Equivalent circuit of a voltage-fed Z-source inverter. Dashed line illustrates the interface between the impedance network and the inverter stage.

3.1.1 Modeling of a voltage-fed Z-source inverter impedance network

When the Z-source inverter operates in continuous conduction mode (CCM), the impedance network may operate in three different states: a) shoot-through state, b) non-shoot-through active state, and c) non-shoot-through zero state (Peng; 2003). During the shoot-through state the switch in the equivalent circuit of the Fig. 3.3 is closed and during the non-shoot-through states the switch is open. Undesired states will occur, if the inductor current or the diode current falls to zero during the non-shoot-through state. In this thesis, only the CCM operation is considered.

a) Shoot-through state

Shoot-through state forces the diode in circuit of Fig. 3.3 to reverse biased conditions. As a result of the equivalent dc-link short-circuit, energy is transferred from impedance network capacitors to impedance network inductors and at the same time the inverter must operate in zero state. According to Fig. 3.3, the inductor voltages u_{L1} and u_{L2} during the shoot-through state are

$$u_{L1} = u_{C2} - (r_{L1} + r_{C2})i_{L1} \quad (3.1)$$

and

$$u_{L2} = u_{C1} - (r_{L2} + r_{C1})i_{L2}, \quad (3.2)$$

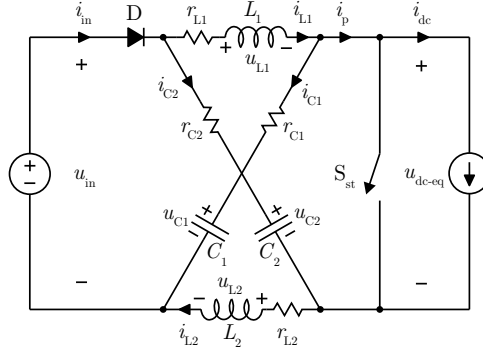


Figure 3.3. Equivalent circuit of a voltage-fed impedance network.

respectively. Correspondingly, since the diode is reverse biased, the capacitor currents are

$$i_{C1} = -i_{L2} \quad (3.3)$$

and

$$i_{C2} = -i_{L1}, \quad (3.4)$$

respectively. The input current i_{in} and the equivalent dc-link voltage u_{dc-eq} of the impedance network are zero during the shoot-through state. In addition, since the inverter operates in zero stage, the current i_{dc} must be zero.

b) Non-shoot-through active state

During the non-shoot-through active state, the inverter stage switch matrix of Fig. 3.2 operates in one of the six active state. Now, the diode in the impedance network is forced to forward bias conditions, and according to Fig. 3.3 the inductor voltages are

$$u_{L1} = u_{in} - U_D - r_D i_D - r_{L1} i_{L1} - r_{C1} i_{C1} - u_{C1} \quad (3.5)$$

and

$$u_{L2} = u_{in} - U_D - r_D i_D - r_{L2} i_{L2} - r_{C2} i_{C2} - u_{C2}, \quad (3.6)$$

where U_D is the diode forward voltage drop and r_D diode on-state resistance. The diode current and the capacitors currents in (3.5) and (3.6) can be computed as a function of the dc-link current and the inductor current, i.e.,

$$i_{C1} = i_{L1} - i_{dc}, \quad (3.7)$$

$$i_{C2} = i_{L2} - i_{dc}, \quad (3.8)$$

and

$$i_D = i_{L1} + i_{C2} = i_{L1} + i_{L2} - i_{dc}. \quad (3.9)$$

Inserting (3.7) - (3.9) to (3.5) and (3.6) yields

$$u_{L1} = u_{in} - u_{C1} - U_D - (r_{L1} + r_{C1} + r_D)i_{L1} - r_D i_{L2} + (r_D + r_{C1})i_{dc} \quad (3.10)$$

and

$$u_{L2} = u_{in} - u_{C2} - U_D - (r_{L2} + r_{C2} + r_D)i_{L2} - r_D i_{L1} + (r_D + r_{C2})i_{dc}. \quad (3.11)$$

During the non-shoot-through active state, energy is transferred from impedance network to the inverter stage. The equivalent dc-link voltage supplying the inverter bridge can be given by

$$u_{dc} = u_{C1} + u_{C2} - u_{in} + U_D - (r_{C1} + r_{C2} + r_D)i_{dc} + (r_{C1} + r_D)i_{L1} + (r_{C2} + r_D)i_{L2} \quad (3.12)$$

and the input current of the network by

$$i_{in} = i_D = i_{L1} + i_{L2} - i_{dc}. \quad (3.13)$$

c) Non-shoot-through zero state

Equations representing the non-shoot-through zero state are the same as in the non-shoot-through active state with the exception that the current flowing to inverter bridge switch matrix i_{dc} is zero. When the inverter bridge current is zero, the inductor voltages and capacitor currents can be given by

$$u_{L1} = u_{in} - u_{C1} - U_D - (r_{L1} + r_{C1} + r_D)i_{L1} - r_D i_{L2} \quad (3.14a)$$

$$u_{L2} = u_{in} - u_{C2} - U_D - (r_{L2} + r_{C2} + r_D)i_{L2} - r_D i_{L1} \quad (3.14b)$$

$$i_{C1} = i_{L1} \quad (3.14c)$$

$$i_{C2} = i_{L2} \quad (3.14d)$$

as well as the equivalent dc-link voltage and the input current by

$$u_{dc} = u_{C1} + u_{C2} - u_{in} + U_D + (r_{C1} + r_D)i_{L1} + (r_{C2} + r_D)i_{L2} \quad (3.15a)$$

$$i_{in} = i_{L1} + i_{L2}. \quad (3.15b)$$

Averaging the operation of the voltage-fed impedance network

The average behavior of the impedance network is found by multiplying the equations describing the shoot-through state sub-circuit with the shoot-through duty cycle d_{st} , and the equations describing the operation during the non-shoot-through state with its complement d'_{st} (in continuous conduction mode, $d'_{st} = 1 - d_{st}$). The average inductor voltages and capacitor currents are proportional to the average inductor currents and capacitor voltages derivatives, respectively, and the average model can be given by

$$L_1 \frac{d\langle i_{L1} \rangle}{dt} = d_{st} \langle u_{C2} \rangle + d'_{st} \langle u_{in} \rangle - d'_{st} \langle u_{C1} \rangle - d'_{st} U_D + (r_D + r_{C1}) \langle i_{dc} \rangle - (d'_{st} (r_{L1} + r_{C1} + r_D) + d_{st} (r_{L1} + r_{C2})) \langle i_{L1} \rangle - d'_{st} r_D \langle i_{L2} \rangle \quad (3.16a)$$

$$L_2 \frac{d\langle i_{L2} \rangle}{dt} = d_{st} \langle u_{C1} \rangle + d'_{st} \langle u_{in} \rangle - d'_{st} \langle u_{C2} \rangle - d'_{st} U_D + (r_D + r_{C2}) \langle i_{dc} \rangle - (d'_{st} (r_{L2} + r_{C2} + r_D) + d_{st} (r_{L2} + r_{C1})) \langle i_{L2} \rangle - d'_{st} r_D \langle i_{L1} \rangle \quad (3.16b)$$

$$C_1 \frac{d\langle u_{C1} \rangle}{dt} = d'_{st} \langle i_{L1} \rangle - d_{st} \langle i_{L2} \rangle - \langle i_{dc} \rangle, \quad (3.16c)$$

$$C_2 \frac{d\langle u_{C2} \rangle}{dt} = -d_{st} \langle i_{L1} \rangle + d'_{st} \langle i_{L2} \rangle - \langle i_{dc} \rangle, \quad (3.16d)$$

The average of the equivalent dc-link voltage may be written as

$$\langle u_{dc} \rangle = \langle u_{C1} \rangle + \langle u_{C2} \rangle - \langle u_{in} \rangle + U_D - (r_{C1} + r_{C2} + r_D) \langle i_{dc} \rangle - (r_{C1} + r_D) \langle i_{L1} \rangle + (r_{C2} + r_D) \langle i_{L2} \rangle \quad (3.17)$$

and the average input current of the impedance network as

$$\langle i_{in} \rangle = d'_{st} \langle i_{L1} \rangle + d'_{st} \langle i_{L2} \rangle - \langle i_{dc} \rangle. \quad (3.18)$$

Steady state operating point

The steady-state operating point of the converter can be solved by setting the time derivatives of the average model in (3.16a) - (3.18) to zero. The steady state values denoted by the uppercase letters of the impedance network currents as a function of the input current are

$$I_{L1} = I_{L2} = I_{in}, \quad I_{dc} = (1 - 2D_{st})I_{in}. \quad (3.19)$$

A reasonable simplification of the circuit is that the impedance network capacitor and inductor ESRs are equal, i.e. $r_{C1} = r_{C2}$ and $r_{L1} = r_{L2}$. With this assumption, the shoot-through duty cycle of the converter as a function of the input voltage, input current, and the impedance network capacitor voltage equals

$$D_{st} = \frac{U_{Cz} - U_{in} + U_D + (r_D + r_{L1})I_{in}}{2U_{Cz} - U_{pv} + U_D - 2r_{C1}I_{in}}, \quad (3.20)$$

where the average impedance network capacitor voltage U_{C1} is denoted by U_{Cz} . When the capacitor ESRs are equal, the average capacitor voltages are also equal, i.e.

$$U_{Cz} = U_{C1} = U_{C2}. \quad (3.21)$$

The steady state value of the equivalent dc-link voltage supplying the inverter stage can be given by

$$U_{dc} = 2U_{Cz} - U_{in} + U_D + (2r_{C1} + r_D)2D_{st}I_{in} + r_D I_{in}. \quad (3.22)$$

If the losses in the impedance network are neglected, the impedance network capacitor voltage and the equivalent dc-link voltage can be given by

$$U_{Cz} = \frac{1 - D_{st}}{1 - 2D_{st}} U_{in} \quad (3.23)$$

and

$$U_{dc} = \frac{1}{1 - 2D_{st}} U_{in} = BU_{in}, \quad (3.24)$$

where B is known as the boost-factor (Peng; 2003). When the shoot-through duty cycle D_{st} is increased, the equivalent dc-link voltage becomes higher than the input voltage. Since according to (3.24) the impedance network cannot be used to decrease the equivalent dc-link voltage below the input voltage, the voltage-buck property of the Z-source inverter is achieved by the control of the voltage-buck-type inverter stage.

Linear model of the voltage-fed impedance network

The derived average model given in (3.16a) - (3.18) is highly nonlinear. The non-linearity is removed by linearizing the operation of the converter at a steady-state operating point by developing the partial derivatives in respect to each input and state variable present in the average model. The linearized model formulated according to the conventional state-space representation can be given by

$$\begin{aligned} s \underbrace{\begin{bmatrix} \hat{i}_{L1} \\ \hat{i}_{L2} \\ \hat{u}_{C1} \\ \hat{u}_{C2} \end{bmatrix}}_x &= \underbrace{\begin{bmatrix} -\frac{R_1}{L_1} & -\frac{D'_{st}r_D}{L_1} & -\frac{D'_{st}}{L_1} & \frac{D_{st}}{L_1} \\ -\frac{D'_{st}r_D}{L_2} & -\frac{R_1}{L_2} & \frac{D_{st}}{L_2} & -\frac{D'_{st}}{L_2} \\ \frac{D'_{st}}{C_1} & -\frac{D_{st}}{C_1} & 0 & 0 \\ -\frac{D_{st}}{C_2} & \frac{D'_{st}}{C_2} & 0 & 0 \end{bmatrix}}_A \underbrace{\begin{bmatrix} \hat{i}_{L1} \\ \hat{i}_{L2} \\ \hat{u}_{C1} \\ \hat{u}_{C2} \end{bmatrix}}_x \\ &+ \underbrace{\begin{bmatrix} \frac{D'_{st}}{L_1} & \frac{r_D+r_{C1}}{L_1} & \frac{U_1}{L_1} \\ \frac{D'_{st}}{L_2} & \frac{r_D+r_{C1}}{L_2} & \frac{U_1}{L_2} \\ 0 & -\frac{1}{C_1} & -\frac{2I_{in}}{C_1} \\ 0 & -\frac{1}{C_2} & -\frac{2I_{in}}{C_2} \end{bmatrix}}_B \underbrace{\begin{bmatrix} \hat{u}_{in} \\ \hat{i}_{dc} \\ \hat{d}_{st} \end{bmatrix}}_u \end{aligned} \quad (3.25)$$

and

$$\underbrace{\begin{bmatrix} \hat{i}_{in} \\ \hat{u}_{dc} \end{bmatrix}}_{\mathbf{y}} = \underbrace{\begin{bmatrix} D'_{st} & D'_{st} & 0 & 0 \\ r_D + r_{C1} & r_D + r_{C1} & 1 & 1 \end{bmatrix}}_{\mathbf{C}} \underbrace{\begin{bmatrix} \hat{i}_{L1} \\ \hat{i}_{L2} \\ \hat{u}_{C1} \\ \hat{u}_{C2} \end{bmatrix}}_{\mathbf{x}} + \underbrace{\begin{bmatrix} 0 & -1 & -2I_{in} \\ -1 & -(2r_{C1} + r_D) & 0 \end{bmatrix}}_{\mathbf{D}} \underbrace{\begin{bmatrix} \hat{u}_{in} \\ \hat{i}_{dc} \\ \hat{d}_{st} \end{bmatrix}}_{\mathbf{u}} \quad (3.26)$$

where

$$\begin{aligned} U_1 &= 2U_{C1} - U_{in} + U_D + 2r_D I_{in} \\ R_1 &= D'_{st} r_D + r_{C1} + r_{L1}. \end{aligned} \quad (3.27)$$

The system input-to-output transfer functions can be then solved from (3.25) and (3.26) by using a matrix manipulation software such as MATLAB applying

$$\mathbf{y} = \mathbf{G}\mathbf{u} \Leftrightarrow \mathbf{G} = \mathbf{C}(\mathbf{s}\mathbf{I} - \mathbf{A})^{-1}\mathbf{B} + \mathbf{D}, \quad (3.28)$$

where the system input-to-output transfer matrix

$$\mathbf{G} = \begin{bmatrix} Y_{in} & T_{oi} & G_{ci} \\ G_{io} & -Z_o & G_{co} \end{bmatrix}. \quad (3.29)$$

Using the derived transfer functions, the input and output dynamics of a voltage-fed impedance may be represented as

$$\hat{i}_{in} = Y_{in}\hat{u}_{in} + T_{oi}\hat{i}_{dc} + G_{ci}\hat{d}_{st} \quad (3.30)$$

and

$$\hat{u}_{dc} = G_{io}\hat{u}_{in} - Z_o\hat{i}_{dc} + G_{co}\hat{d}_{st}, \quad (3.31)$$

respectively. The resulting linear two-port model is shown in Fig. 3.4.

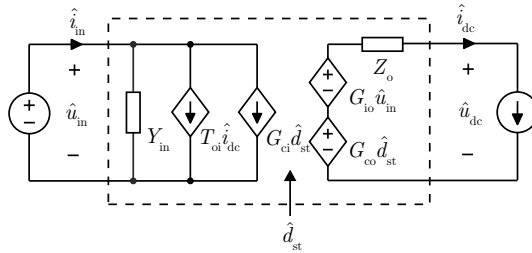


Figure 3.4. Linear model of a voltage-fed impedance network

If the parasitic components are neglected and the impedance network is assumed to be ideal, the set of transfer functions describing the open-loop dynamics of the voltage-fed impedance network can be given by:

$$Y_{\text{in}} = \frac{1}{\Delta^{\text{vf}}} \frac{2D_{\text{st}}'^2 s}{L_1} \quad (3.32\text{a})$$

$$T_{\text{oi}} = \left(\frac{1}{\Delta^{\text{vf}}} \frac{2(1 - 2D_{\text{st}})D_{\text{st}}'}{C_1 L_1} - 1 \right) \quad (3.32\text{b})$$

$$G_{\text{ci}} = -\frac{1}{\Delta^{\text{vf}}} 2D_{\text{st}}' \frac{2I_{\text{in}}}{L_1 C_1} \left(1 - \frac{s}{\omega_{\text{zero-in}}} \right) - 2I_{\text{in}} \quad (3.32\text{c})$$

$$G_{\text{io}} = \left(\frac{1}{\Delta^{\text{vf}}} \frac{2(1 - 2D_{\text{st}})D_{\text{st}}'}{L_1 C_1} - 1 \right) \quad (3.32\text{d})$$

$$Z_{\text{o}} = \frac{1}{\Delta^{\text{vf}}} \frac{2s}{C_1} \quad (3.32\text{e})$$

$$G_{\text{co}} = \frac{1}{\Delta^{\text{vf}}} \frac{2(1 - 2D_{\text{st}})U_{\text{dc}}}{L_1 C_1} \left(1 - \frac{s}{\omega_{\text{zero-out}}} \right), \quad (3.32\text{f})$$

where the right-half-plane zeros associated with the control-to-input and the control-to-output transfer functions are

$$\omega_{\text{zero-in}} = \frac{2I_{\text{in}}}{U_{\text{dc}} C_1}, \quad \omega_{\text{zero-out}} = \frac{(1 - 2D_{\text{st}})U_{\text{dc}}}{2I_{\text{in}} L_1}, \quad (3.33)$$

respectively, and the characteristic polynomial of a voltage-fed system is

$$\Delta^{\text{vf}} = s^2 + \omega_{\text{res}}^2, \quad (3.34)$$

where

$$\omega_{\text{res}} = \sqrt{\frac{1 - 4D_{\text{st}}D_{\text{st}}'}{L_1 C_1}}. \quad (3.35)$$

According to (3.32a) - (3.35), the ideal impedance network is a second-order system, having an operating-point-dependent resonant frequency and right-half-plane zeros in the control dynamics.

In Z-source inverter, the inductor current and/or the capacitor voltage may be also taken as a feedback variable. To analyze the dynamics associated with the state variables, the input-to-state transfer functions are found by solving the state-transition matrix Φ as shown in (3.36).

$$\mathbf{x} = \Phi \mathbf{u} \Leftrightarrow \Phi = (s\mathbf{I} - \mathbf{A})^{-1} \mathbf{B}, \quad (3.36)$$

where

$$\Phi = \begin{bmatrix} G_{\text{iL1}} & G_{\text{oL1}} & G_{\text{cL1}} \\ G_{\text{iL2}} & G_{\text{oL2}} & G_{\text{cL2}} \\ G_{\text{iC1}} & G_{\text{oC1}} & G_{\text{cC1}} \\ G_{\text{iC2}} & G_{\text{oC2}} & G_{\text{cC2}} \end{bmatrix}. \quad (3.37)$$

In this thesis, the dynamics of the impedance network capacitor voltage C_1 is of interest, since it is taken as a feedback variable in the control system analyzed later. The transfer functions associated to impedance network capacitor voltage by using the transfer functions given in (3.37) equal

$$\hat{u}_{Cz} = G_{iC1}(1 + sr_{C1}C_1)\hat{u}_{in} + G_{oC1}(1 + sr_{C1}C_1)\hat{i}_{dc} + G_{cC1}(1 + sr_{C1}C_1)\hat{d}_{st}, \quad (3.38)$$

where the effect of the equivalent series resistance of the capacitor is included. For further analysis, the transfer functions in (3.38) are rewritten as

$$\hat{u}_{Cz} = G_{iCz}\hat{u}_{in} + G_{oCz}\hat{i}_{dc} + G_{cCz}\hat{d}_{st}. \quad (3.39)$$

Unfortunately, the capacitor voltage is an internal stage variable (not an electrical terminal), and is thus not visible in the two-port network describing the input-output characteristics.

3.1.2 Modeling of a current-fed Z-source inverter impedance network

The current-fed Z-source inverter is shown in Fig. 3.5. As in case of the voltage-fed inverter, the inverter is divided into two systems: the impedance network and the inverter stage. The impedance network affecting the behavior of the inverter stage is shown in Fig. 3.6. As the voltage-fed Z-source inverter, also the impedance network of the current-fed Z-source inverter operating in continuous conduction mode has three states: a) shoot-through state, b) non-shoot-through active state, and c) the non-shoot-through zero state, which are commanded by the control of the inverter bridge.

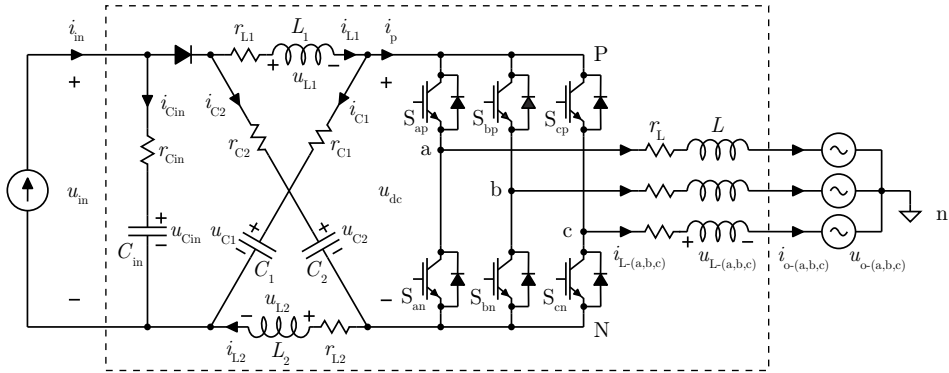


Figure 3.5. Current-fed Z-source inverter.

a) Shoot-through state

During the shoot-through state the diode disconnects the input capacitor from the X-shaped impedance network. The energy is transferred from the capacitors to the inductors, and according to circuit diagram of Fig. 3.6, the inductor voltages can be given by

$$u_{L1} = u_{C2} - (r_{L1} + r_{C2})i_{L1} \quad (3.40)$$

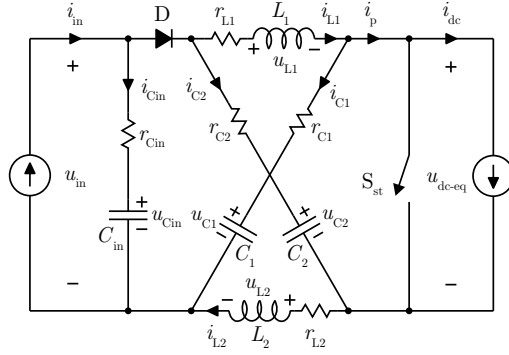


Figure 3.6. Current-fed impedance network

and

$$u_{L2} = u_{C1} - (r_{L2} + r_{C1})i_{L2}. \quad (3.41)$$

Correspondingly, the impedance network capacitors currents can be given by

$$i_{C1} = -i_{L2} \quad (3.42)$$

and

$$i_{C2} = -i_{L1}. \quad (3.43)$$

The current-fed impedance network has one additional memory element compared to the voltage-fed impedance network, the input capacitor. Since the diode is reverse biased, the current of the input capacitor equals the input current of the converter, i.e.

$$i_{in} = i_{Cin} = C_{in} \frac{du_{Cin}}{dt}. \quad (3.44)$$

The input voltage of the converter during the shoot-through state is

$$u_{in} = u_{Cin} + r_{Cin}i_{in}. \quad (3.45)$$

b) Non-shoot-through active state

During the active state, the diode in the impedance network is forward biased, and according to Fig. 3.6 the inductor voltages can be given by

$$u_{L1} = u_{in} - U_D - r_D i_D - r_{L1} i_{L1} - r_{C1} i_{C1} - u_{C1} \quad (3.46)$$

and

$$u_{L2} = u_{in} - U_D - r_D i_D - r_{L2} i_{L2} - r_{C2} i_{C2} - u_{C2}, \quad (3.47)$$

where U_D is the diode forward voltage drop and r_D diode on-state resistance. The capacitor currents and diode current in (3.46) and (3.47) can be given by

$$i_{C1} = i_{L1} - i_{dc}, \quad (3.48)$$

$$i_{C2} = i_{L2} - i_{dc} \quad (3.49)$$

and

$$i_D = i_{L1} + i_{C2} = i_{L1} + i_{L2} - i_{dc}. \quad (3.50)$$

During the non-shoot-through state, the input voltage of the impedance network can be given by

$$u_{in} = u_{Cin} + r_{Cin}i_{in} - r_{Cin}i_{L1} - r_{Cin}i_{L2} + r_{Cin}i_{dc}. \quad (3.51)$$

Inserting (3.48) - (3.50) and (3.51) into (3.46) and (3.47) yields

$$\begin{aligned} u_{L1} = & u_{Cin} - u_{C1} - U_D - (r_{L1} + r_{C1} + r_D + r_{Cin})i_{L1} - (r_D + r_{Cin})i_{L2} \\ & + (r_D + r_{C1} + r_{Cin})i_{dc} + r_{Cin}i_{in} \end{aligned} \quad (3.52)$$

and

$$\begin{aligned} u_{L2} = & u_{Cin} - u_{C2} - U_D - (r_{L2} + r_{C2} + r_D + r_{Cin})i_{L2} - (r_D + r_{Cin})i_{L1} \\ & + (r_D + r_{C2} + r_{Cin})i_{dc} + r_{Cin}i_{in}. \end{aligned} \quad (3.53)$$

During the non-shoot-through state, the impedance network capacitor and input capacitor currents are

$$i_{C1} = i_{L1} - i_{dc}, \quad (3.54)$$

$$i_{C2} = i_{L2} - i_{dc} \quad (3.55)$$

and

$$i_{Cin} = i_{in} - i_{L1} - i_{L2} + i_{dc}. \quad (3.56)$$

Finally, the equivalent dc-link voltage during the non-shoot-through state can be given by

$$\begin{aligned} u_{dc} = & u_{C1} + u_{C2} - u_{Cin} + U_D + (r_{C1} + r_D + r_{Cin})i_{L1} + (r_{C2} + r_D + r_{Cin})i_{L2} \\ & - (r_{C1} + r_{C2} + r_D + r_{Cin})i_{dc} - r_{Cin}i_{in}. \end{aligned} \quad (3.57)$$

c) Non-shoot-through zero state

The equations corresponding to the non-shoot-through zero stage and given in (3.58a) - (3.58g) are the same as the equations of the non-shoot-through active state given above with the exception that the output current of the network is zero.

$$\begin{aligned} u_{L1} = & u_{Cin} - u_{C1} - U_D - (r_{L1} + r_{C1} + r_D + r_{Cin})i_{L1} - (r_D + r_{Cin})i_{L2} \\ & + (r_D + r_{C1} + r_{Cin})i_{dc} + r_{Cin}i_{in} \end{aligned} \quad (3.58a)$$

$$u_{L2} = u_{Cin} - u_{C2} - U_D - (r_{L2} + r_{C2} + r_D + r_{Cin})i_{L2} - (r_D + r_{Cin})i_{L1} \\ + (r_D + r_{C2} + r_{Cin})i_{dc} + r_{Cin}i_{in}. \quad (3.58b)$$

$$i_{C1} = i_{L1} \quad (3.58c)$$

$$i_{C2} = i_{L2} \quad (3.58d)$$

$$i_{Cin} = i_{in} - i_{L1} - i_{L2} \quad (3.58e)$$

$$u_{in} = u_{Cin} + r_{Cin}i_{in} - r_{Cin}i_{L1} - r_{Cin}i_{L2} \quad (3.58f)$$

$$u_{dc} = u_{C1} + u_{C2} - u_{Cin} + U_D + (r_{C1} + r_D + r_{Cin})i_{L1} + (r_{C2} + r_D + r_{Cin})i_{L2} \\ - r_{Cin}i_{in}. \quad (3.58g)$$

Averaging the operation of the current-fed impedance network

As in voltage-fed impedance network, the average behavior of the network is found by multiplying the equations describing the shoot-through state sub circuit with the shoot-through duty cycle d_{st} , and the equations describing the operation during the non-shoot-through state with its complement d'_{st} . In continuous conduction mode, $d'_{st} = 1 - d_{st}$, and the average model can be given by

$$L_1 \frac{d\langle i_{L1} \rangle}{dt} = d_{st}\langle u_{C2} \rangle + d'_{st}\langle u_{Cin} \rangle - d'_{st}\langle u_{C1} \rangle - d'_{st}U_D + (r_D + r_{C1} + r_{Cin})\langle i_{dc} \rangle + d'_{st}r_{Cin}\langle i_{in} \rangle \\ - (d'_{st}(r_{L1} + r_{C1} + r_D + r_{Cin}) + d_{st}(r_{L1} + r_{C2}))\langle i_{L1} \rangle - d'_{st}(r_D + r_{Cin})\langle i_{L2} \rangle \quad (3.59a)$$

$$L_2 \frac{d\langle i_{L2} \rangle}{dt} = d_{st}\langle u_{C1} \rangle + d'_{st}\langle u_{Cin} \rangle - d'_{st}\langle u_{C2} \rangle - d'_{st}U_D + (r_D + r_{C2} + r_{Cin})\langle i_{dc} \rangle + d'_{st}r_{Cin}\langle i_{in} \rangle \\ - (d'_{st}(r_{L2} + r_{C2} + r_D + r_{Cin}) + d_{st}(r_{L2} + r_{C1}))\langle i_{L2} \rangle - d'_{st}(r_D + r_{Cin})\langle i_{L1} \rangle \quad (3.59b)$$

$$C_1 \frac{d\langle u_{C1} \rangle}{dt} = d'_{st}\langle i_{L1} \rangle - d_{st}\langle i_{L2} \rangle - \langle i_{dc} \rangle \quad (3.59c)$$

$$C_2 \frac{d\langle u_{C2} \rangle}{dt} = -d_{st}\langle i_{L1} \rangle + d'_{st}\langle i_{L2} \rangle - \langle i_{dc} \rangle \quad (3.59d)$$

$$C_{in} \frac{d\langle u_{Cin} \rangle}{dt} = \langle i_{in} \rangle - d'_{st}\langle i_{L1} \rangle - d'_{st}\langle i_{L2} \rangle + \langle i_{dc} \rangle. \quad (3.59e)$$

Using the same procedure, the average behavior of the input and the output terminal can be given by

$$\langle u_{in} \rangle = r_{Cin}\langle i_{in} \rangle + \langle u_{Cin} \rangle - r_{Cin}d'_{st}\langle i_{L1} \rangle - r_{Cin}d'_{st}\langle i_{L2} \rangle + r_{Cin}\langle i_{dc} \rangle \quad (3.60a)$$

$$\langle u_{dc} \rangle = \langle u_{C1} \rangle + \langle u_{C2} \rangle - \langle u_{Cin} \rangle + U_D - (r_{C1} + r_{C2} + r_D + r_{Cin})\langle i_{dc} \rangle \\ + (r_{C1} + r_D + r_{Cin})\langle i_{L1} \rangle + (r_{C2} + r_D + r_{Cin})\langle i_{L2} \rangle - r_{Cin}\langle i_{in} \rangle. \quad (3.60b)$$

Steady state operating point of the current-fed impedance network

Steady-state operating point of the converter may be solved by setting the time derivatives of the average model in (3.59a) - (3.60b) to zero. The steady-state values of the impedance network currents as a function of the input current are

$$I_{L1} = I_{L2} = I_{in}, \quad I_{dc} = (1 - 2D_{st})I_{in}. \quad (3.61)$$

A reasonable simplification of the circuit is, that the impedance network capacitor and inductor ESRs are equal, i.e. $r_{C1} = r_{C2}$ and $r_{L1} = r_{L2}$. With this assumption, the shoot-through duty cycle of the converter as a function of the input voltage, input current, and the impedance network capacitor voltage equals

$$D_{st} = \frac{U_{Cz} - U_{in} + U_D + (r_D + r_{L1})I_{in}}{2U_{Cz} - U_{pv} + U_D - (2r_{C1} + r_{Cin})I_{in}}, \quad (3.62)$$

where the average impedance network capacitor voltage U_{C1} is denoted by U_{Cz} . When the capacitor ESRs are equal, the average capacitor voltages are also equal, i.e.

$$U_{Cz} = U_{C1} = U_{C2}. \quad (3.63)$$

The output voltage of the current-fed impedance network, i.e. the steady-state value of the equivalent dc-link voltage, equals

$$U_{dc} = 2C_{Cz} - U_{in} + U_D + (2r_{C1} + r_D + r_{Cin})2D_{st}I_{in} + r_D I_{in}. \quad (3.64)$$

If the input capacitor equivalent series resistance is neglected, the steady state values of the current-fed impedance network given in (3.61) - (3.64) are the same as the value of the voltage-fed impedance network given in (3.19) - (3.22).

Linearized average model of the current-fed impedance network

The linearized model of a current-fed impedance network formulated into a conventional state-space representation can be written as follows

$$\begin{aligned} \underbrace{\begin{bmatrix} \hat{i}_{L1} \\ \hat{i}_{L2} \\ \hat{u}_{C1} \\ \hat{u}_{C2} \\ \hat{u}_{Cin} \end{bmatrix}}_x &= \underbrace{\begin{bmatrix} -\frac{R_1}{L_1} & -\frac{D'_{st}(r_D+r_{Cin})}{L_1} & -\frac{D'_{st}}{L_1} & \frac{D_{st}}{L_1} & \frac{D'_{st}}{L_1} \\ -\frac{D'_{st}(r_D+r_{Cin})}{L_2} & -\frac{R_1}{L_2} & \frac{D_{st}}{L_2} & -\frac{D'_{st}}{L_2} & \frac{D'_{st}}{L_2} \\ \frac{D'_{st}}{C_1} & -\frac{D_{st}}{C_1} & 0 & 0 & 0 \\ -\frac{D_{st}}{C_2} & \frac{D'_{st}}{C_2} & 0 & 0 & 0 \\ -\frac{D'_{st}}{C_{in}} & -\frac{D_{st}}{C_{in}} & 0 & 0 & 0 \end{bmatrix}}_A \underbrace{\begin{bmatrix} \hat{i}_{L1} \\ \hat{i}_{L2} \\ \hat{u}_{C1} \\ \hat{u}_{C2} \\ \hat{u}_{Cin} \end{bmatrix}}_x \\ &+ \underbrace{\begin{bmatrix} \frac{D'_{st}r_{Cin}}{L_1} & \frac{r_D+r_{C1}+r_{Cin}}{L_1} & \frac{U_1}{L_1} \\ \frac{D'_{st}r_{Cin}}{L_2} & \frac{r_D+r_{C1}+r_{Cin}}{L_2} & \frac{U_1}{L_2} \\ 0 & -\frac{1}{C_1} & -\frac{2I_{in}}{C_1} \\ 0 & -\frac{1}{C_2} & -\frac{2I_{in}}{C_2} \\ \frac{1}{C_{in}} & \frac{1}{C_{in}} & \frac{2I_{in}}{C_{in}} \end{bmatrix}}_B \underbrace{\begin{bmatrix} \hat{i}_{in} \\ \hat{i}_{dc} \\ \hat{d}_{st} \end{bmatrix}}_u \end{aligned} \quad (3.65a)$$

and

$$\underbrace{\begin{bmatrix} \hat{u}_{\text{in}} \\ \hat{u}_{\text{dc}} \end{bmatrix}}_{\mathbf{y}} = \underbrace{\begin{bmatrix} -D'_{\text{st}} r_{\text{Cin}} & -D'_{\text{st}} r_{\text{Cin}} & 0 & 0 & 1 \\ r_{\text{D}} + r_{\text{C1}} + r_{\text{Cin}} & r_{\text{D}} + r_{\text{C1}} + r_{\text{Cin}} & 1 & 1 & -1 \end{bmatrix}}_{\mathbf{C}} \underbrace{\begin{bmatrix} \hat{i}_{\text{L1}} \\ \hat{i}_{\text{L2}} \\ \hat{u}_{\text{C1}} \\ \hat{u}_{\text{C2}} \\ \hat{u}_{\text{Cin}} \end{bmatrix}}_{\mathbf{x}} + \underbrace{\begin{bmatrix} r_{\text{Cin}} & r_{\text{Cin}} & 2r_{\text{Cin}} I_{\text{in}} \\ -r_{\text{Cin}} & -(2r_{\text{C1}} + r_{\text{D}} + r_{\text{Cin}}) & 0 \end{bmatrix}}_{\mathbf{D}} \underbrace{\begin{bmatrix} \hat{i}_{\text{in}} \\ \hat{i}_{\text{dc}} \\ \hat{d}_{\text{st}} \end{bmatrix}}_{\mathbf{u}}, \quad (3.65\text{b})$$

where

$$\begin{aligned} U_1 &= 2U_{C1} - U_{\text{in}} + U_{\text{D}} + (2r_{\text{D}} + r_{\text{Cin}})I_{\text{in}} \\ R_1 &= D'_{\text{st}}(r_{\text{D}} + r_{\text{Cin}}) + r_{\text{C1}} + r_{\text{L1}}. \end{aligned} \quad (3.66)$$

The state-space model is then used to solve the transfer function matrix given in (3.67) of the current-fed impedance network.

$$\mathbf{G} = \begin{bmatrix} Z_{\text{in}} & T_{\text{oi}} & G_{\text{ci}} \\ G_{\text{io}} & -Z_{\text{o}} & G_{\text{co}} \end{bmatrix}. \quad (3.67)$$

Using the derived transfer functions, the input and the output dynamics may be represented as follows:

$$\hat{u}_{\text{in}} = Z_{\text{in}}\hat{i}_{\text{in}} + T_{\text{oi}}\hat{i}_{\text{dc}} + G_{\text{ci}}\hat{d}_{\text{st}} \quad (3.68)$$

and

$$\hat{u}_{\text{dc}} = G_{\text{io}}\hat{i}_{\text{in}} - Z_{\text{o}}\hat{i}_{\text{dc}} + G_{\text{co}}\hat{d}_{\text{st}}, \quad (3.69)$$

which can be also depicted using the linear two-port shown in Fig. 3.15.

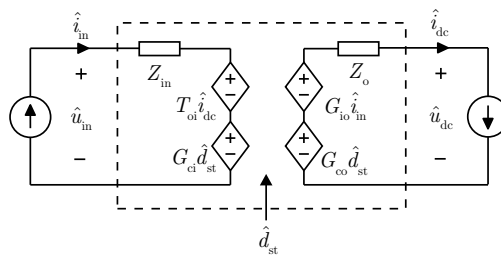


Figure 3.7. Linear model of a current-fed impedance network

If the parasitic components are neglected and the impedance network is assumed to be ideal, the set of transfer functions describing the open-loop dynamics of the current-fed impedance network can be written as follows:

$$Z_{\text{in}} = \frac{1}{\Delta_{\text{cf}}} \left(s^2 + \frac{(2D_{\text{st}} - 1)^2}{L_1 C_1} \right) \frac{1}{C_{\text{in}}} \quad (3.70\text{a})$$

$$T_{oi} = \frac{1}{\Delta^{cf}} \left(\frac{s^2 L_1 C_1 + (2D_{st} - 1)}{L_1 C_1 C_{in}} \right) \quad (3.70b)$$

$$G_{ci} = \frac{1}{\Delta^{cf}} \frac{2}{C_{in} L_1 C_1} (s^2 I_{in} L_1 C_1 - s D'_{st} U_{dc} C_1 + (2D_{st} - 1) I_{in}) \quad (3.70c)$$

$$G_{io} = -\frac{1}{\Delta^{cf}} \left(\frac{s^2 L_1 C_1 + (2D_{st} - 1)}{L_1 C_1 C_{in}} \right) \quad (3.70d)$$

$$Z_o = \frac{1}{\Delta^{cf}} \left(\frac{s^2 (2L_1 C_{in} + L_1 C_1) + (2D_{st} - 1) + 2D'_{st}}{L_1 C_1 C_{in}} \right) \quad (3.70e)$$

$$G_{co} = -\frac{1}{\Delta^{cf}} \frac{1}{L_1 C_1 C_{in}} \left((4C_{in} + L_1 C_1) I_{in} s^2 + (D'_{st} C_1 - 2(1 - 2D_{st}) C_{in}) U_{dc} s + ((2D_{st} - 1) - 4D'_{st}) I_{in} \right), \quad (3.70f)$$

where the characteristic polynomial of the system equals

$$\Delta^{cf} = s \left(s^2 + \frac{2D_{st}'^2 C_1 + C_{in} (2D_{st} - 1)^2}{C_{in} C_1 L_1} \right). \quad (3.71)$$

The dynamics of the ideal current-fed impedance network are third order, and the location of the resonance depends on the operating point of the inverter.

As in the voltage-fed impedance network, the inductor current and/or the capacitor voltage may be also taken as a feedback variable. The input-to-state transfer functions are found by solving the state-transition matrix of the current-fed system and including the effect of the equivalent series resistances as shown previously in (3.36) - (3.39).

3.1.3 Comparison of current-fed and voltage-fed ZSI dynamic characteristics

To compare the characteristics of a voltage-fed and a current-fed Z-source inverter, first a method to include the effect of the impedance network to the inverter dynamics must be derived.

Voltage-fed Z-source inverter

The voltage-fed impedance network model can be combined with the model of the voltage-fed VSI-based inverter model as shown in Fig. 3.8.

When the source subsystem (the impedance network) and the load subsystem (the VSI-based inverter) are interconnected, the new system input variables are the input current of the impedance network \hat{i}_{in} , output voltage of the inverter stage (i.e. the grid voltage) \hat{u}_o , shoot-through duty cycle of the impedance network \hat{d}_{st} , and duty ratio of the inverter stage \hat{d} . The dc-link current \hat{i}_{dc} and the dc-link \hat{u}_{dc} are the internal state-variables (intermediate variables) of the system.

$$\begin{bmatrix} \hat{i}_{in} \\ \hat{i}_o \\ \hat{i}_o \end{bmatrix} = \begin{bmatrix} \mathbf{Y}_{in}^{vf-zsi} & \mathbf{T}_{oi}^{vf-zsi} & \mathbf{G}_{ci}^{vf-zsi} & \mathbf{G}_{sti}^{vf-zsi} \\ \mathbf{G}_{io}^{vf-zsi} & -\mathbf{Y}_o^{vf-zsi} & \mathbf{G}_{co}^{vf-zsi} & \mathbf{G}_{sto}^{vf-zsi} \end{bmatrix} \begin{bmatrix} \hat{u}_{in} \\ \hat{u}_o \\ \hat{d} \\ \hat{d}_{st} \end{bmatrix}, \quad (3.72)$$

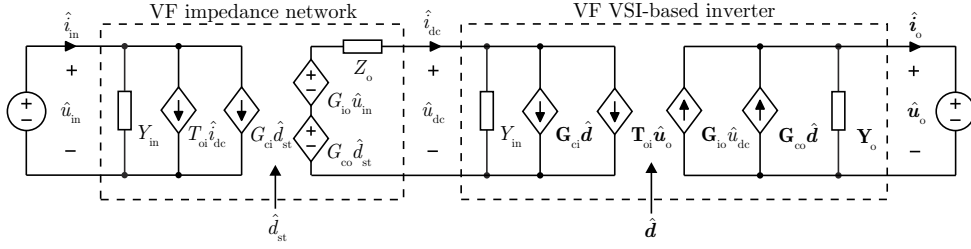


Figure 3.8. Linear model of a voltage-fed ZSI-based inverter.

The input to output transfer functions of the voltage-fed ZSI in (3.72) are

$$Y_{in}^{vf-zsi} = Y_{in}^{vf-zn} + T_{oi}^{vf-zn} \frac{Y_{in}^{vsi} G_{io}^{vf-zn}}{1 + Z_o^{vf-zn} Y_{in}^{vsi}} \quad (3.73a)$$

$$T_{oi}^{vf-zsi} = T_{oi}^{vf-zn} \frac{1}{1 + Y_{in}^{vsi} Z_o^{vf-zn}} T_{oi}^{vsi} \quad (3.73b)$$

$$G_{ci}^{vf-zsi} = T_{oi}^{vf-zn} \frac{1}{1 + Y_{in}^{vsi} Z_o^{vf-zn}} G_{ci}^{vsi} \quad (3.73c)$$

$$G_{sti}^{vf-zsi} = G_{ci}^{vf-zn} + T_{oi}^{vf-zn} \frac{Y_{in}^{vsi} G_{co}^{vf-zn}}{1 + Z_o^{vf-zn} Y_{in}^{vsi}} \quad (3.73d)$$

$$G_{io}^{vf-zsi} = G_{io}^{vsi} \frac{G_{io}^{vf-zn}}{1 + Y_{in}^{vsi} Z_o^{vf-zn}} \quad (3.73e)$$

$$Y_o^{vf-zsi} = Y_o^{vsi} + G_{io}^{vsi} \frac{Z_o^{vf-zn}}{1 + Y_{in}^{vsi} Z_o^{vf-zn}} T_{oi}^{vsi} \quad (3.73f)$$

$$G_{co}^{vf-zsi} = G_{co}^{vsi} - G_{io}^{vsi} \frac{Z_o^{vf-zn}}{1 + Y_{in}^{vsi} Z_o^{vf-zn}} G_{ci}^{vsi} \quad (3.73g)$$

$$G_{sto}^{vf-zsi} = G_{io}^{vsi} \frac{G_{co}^{vf-zn}}{1 + Y_{in}^{vsi} Z_o^{vf-zn}} \quad (3.73h)$$

where the superscript 'vf-zn' is added to indicate transfer functions related to the voltage-fed impedance network given in (3.29) and 'vsi' to the VSI-based inverter bridge given in (2.12). In the ZSI, the transfer functions from inputs to impedance network capacitor voltage in (3.74) is also required, since the capacitor voltage is taken as a feedback variable.

$$\begin{bmatrix} \hat{u}_{Cz} \end{bmatrix} = \begin{bmatrix} G_{iCz}^{vf-zsi} & G_{oCz}^{vf-zsi} & G_{cCz}^{vf-zsi} & G_{stCz}^{vf-zsi} \end{bmatrix} \begin{bmatrix} \hat{u}_{in} & \hat{u}_o & \hat{d} & \hat{c} \end{bmatrix}^T, \quad (3.74)$$

where

$$G_{iCz}^{vf-zsi} = G_{iCz}^{vf-zn} + G_{oCz}^{vf-zn} \frac{Y_{in}^{vsi} G_{io}^{vf-zn}}{1 + Z_o^{vf-zn} Y_{in}^{vsi}} \quad (3.75a)$$

$$G_{oCz}^{vf-zsi} = G_{oCz}^{vf-zn} \frac{1}{1 + Y_{in}^{vsi} Z_o^{vf-zn}} T_{oi}^{vsi} \quad (3.75b)$$

$$\mathbf{G}_{cCz}^{vf-zsi} = G_{oCz}^{vf-zn} \frac{1}{1 + Y_{in}^{vsi} Z_o^{vf-zn}} \mathbf{G}_{ci}^{vsi} \quad (3.75c)$$

$$G_{stCz}^{vf-zsi} = G_{cCz}^{vf-zn} + G_{oCz}^{vf-zn} \frac{Y_{in}^{vsi} G_{co}^{vf-zn}}{1 + Z_o^{vf-zn} Y_{in}^{vsi}}. \quad (3.75d)$$

The capacitor voltage is an internal state variable (not an electrical terminal) and is thus not visible in the two-port network shown in Fig. 3.8 describing the input-output characteristics.

Current-fed Z-source inverter

In a current-fed inverter, the overall dynamics can be obtained by combining the model of the current-fed impedance network and the voltage-fed inverter as illustrated in Fig 3.9.

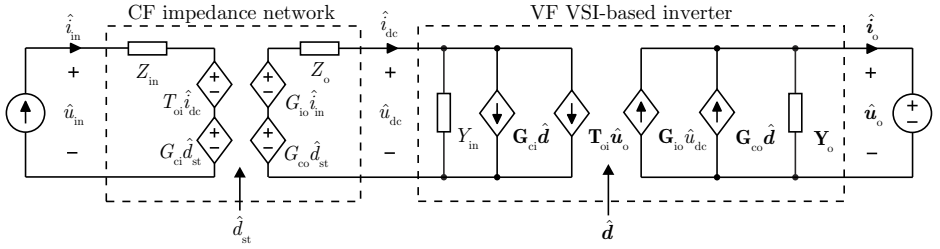


Figure 3.9. Linear model of a current-fed ZSI-based inverter.

The dynamics of the interconnected system can be given by

$$\begin{bmatrix} \hat{u}_{in} \\ \hat{i}_o \end{bmatrix} = \begin{bmatrix} Z_{in}^{cf-zsi} & \mathbf{T}_{oi}^{cf-zsi} & \mathbf{G}_{ci}^{cf-zsi} & G_{sti}^{cf-zsi} \\ \mathbf{G}_{io}^{cf-zsi} & -\mathbf{Y}_o^{cf-zsi} & \mathbf{G}_{co}^{cf-zsi} & G_{sto}^{cf-zsi} \end{bmatrix} \begin{bmatrix} \hat{i}_{in} \\ \hat{u}_o \\ \hat{d} \\ \hat{d}_{st} \end{bmatrix}, \quad (3.76)$$

where the input-to-output transfer functions can be given by

$$Z_{in}^{cf-zsi} = Z_{in}^{cf-zn} + T_{oi}^{cf-zn} \frac{Y_{in}^{vsi} G_{io}^{cf-zn}}{1 + Z_o^{cf-zn} Y_{in}^{vsi}} \quad (3.77a)$$

$$\mathbf{T}_{oi}^{cf-zsi} = T_{oi}^{cf-zn} \frac{1}{1 + Y_{in}^{vsi} Z_o^{cf-zn}} \mathbf{T}_{oi}^{vsi} \quad (3.77b)$$

$$\mathbf{G}_{ci}^{cf-zsi} = T_{oi}^{cf-zn} \frac{1}{1 + Y_{in}^{vsi} Z_o^{cf-zn}} \mathbf{G}_{ci}^{vsi} \quad (3.77c)$$

$$G_{sti}^{cf-zsi} = G_{ci}^{cf-zn} + T_{oi}^{cf-zn} \frac{Y_{in}^{vsi} G_{co}^{cf-zn}}{1 + Z_o^{cf-zn} Y_{in}^{vsi}} \quad (3.77d)$$

$$\mathbf{G}_{io}^{cf-zsi} = \mathbf{G}_{io}^{vsi} \frac{G_{io}^{cf-zn}}{1 + Y_{in}^{vsi} Z_o^{cf-zn}} \quad (3.77e)$$

$$\mathbf{Y}_o^{\text{cf-zsi}} = \mathbf{Y}_o^{\text{vsi}} + \mathbf{G}_{io}^{\text{vsi}} \frac{Z_o^{\text{cf-zn}}}{1 + Y_{in}^{\text{vsi}} Z_o^{\text{cf-zn}}} \mathbf{T}_{oi}^{\text{vsi}} \quad (3.77f)$$

$$\mathbf{G}_{co}^{\text{cf-zsi}} = \mathbf{G}_{co}^{\text{vsi}} - \mathbf{G}_{io}^{\text{vsi}} \frac{Z_o^{\text{cf-zn}}}{1 + Y_{in}^{\text{vsi}} Z_o^{\text{cf-zn}}} \mathbf{G}_{ci}^{\text{vsi}} \quad (3.77g)$$

$$\mathbf{G}_{sto}^{\text{vf-zsi}} = \mathbf{G}_{io}^{\text{vsi}} \frac{G_{co}^{\text{cf-zn}}}{1 + Y_{in}^{\text{vsi}} Z_o^{\text{cf-zn}}} \quad (3.77h)$$

The superscript 'cf-zn' is added to indicate the transfer functions related to the current-fed impedance network given in (3.67) and 'vsi' to the VSI-based inverter bridge given in (2.12). In the ZSI, the transfer functions from inputs-to-state are also required, since the capacitor voltage is taken as a feedback variable. The dynamics associated to the impedance network capacitor can be given by

$$\begin{bmatrix} \hat{u}_{Cz} \end{bmatrix} = \begin{bmatrix} G_{iCz}^{\text{cf-zsi}} & G_{oCz}^{\text{cf-zsi}} & G_{cCz}^{\text{cf-zsi}} & G_{stCz}^{\text{cf-zsi}} \end{bmatrix} \begin{bmatrix} \hat{i}_{in} & \hat{u}_o & \hat{d} & \hat{c} \end{bmatrix}^T, \quad (3.78)$$

where

$$G_{iCz}^{\text{cf-zsi}} = G_{iCz}^{\text{cf-zn}} + G_{oCz}^{\text{cf-zn}} \frac{Y_{in}^{\text{vsi}} G_{io}^{\text{cf-zn}}}{1 + Z_o^{\text{cf-zn}} Y_{in}^{\text{vsi}}} \quad (3.79)$$

$$G_{oCz}^{\text{cf-zsi}} = G_{oCz}^{\text{cf-zn}} \frac{1}{1 + Y_{in}^{\text{vsi}} Z_o^{\text{cf-zn}}} \mathbf{T}_{oi}^{\text{vsi}} \quad (3.80)$$

$$G_{cCz}^{\text{cf-zsi}} = G_{oCz}^{\text{cf-zn}} \frac{1}{1 + Y_{in}^{\text{vsi}} Z_o^{\text{cf-zn}}} \mathbf{G}_{ci}^{\text{vsi}} \quad (3.81)$$

$$G_{stCz}^{\text{cf-zsi}} = G_{cCz}^{\text{cf-zn}} + G_{oCz}^{\text{cf-zn}} \frac{Y_{in}^{\text{vsi}} G_{co}^{\text{cf-zn}}}{1 + Z_o^{\text{cf-zn}} Y_{in}^{\text{vsi}}} \quad (3.82)$$

Comparison of current-fed and voltage-fed ZSI dynamic characteristics

Since the type of the voltage-fed and current-fed model input terminal are different, some of the transfer functions (e.g. T_{oi} , G_{io} and G_{ci}) are not associated with the same electrical quantities, thus only the comparison between the transfer functions that have the same input and output variables are reasonable. The comparison is carried out by comparing the frequency responses (bode plots) produced by using the model presented in previous sections and the parameter values given in Table 1.

To provide explanation how the impedance network stage affects the inverter stage, the impedance characteristics of the voltage-fed and current-fed impedance network input and output terminal are presented in Figs. 3.10a and Fig. 3.10b, respectively. According to the presented frequency responses and transfer functions given in (3.32) and (3.70), the current-fed impedance network clearly is a third order system having an additional resonant term in the input and output impedance compared to the voltage-fed network having second-order dynamics. In addition, the low-frequency value of the current-fed network output impedance is dictated by the input capacitor, whereas in voltage-fed network it is zero due to ideal voltage source present at the input terminal.

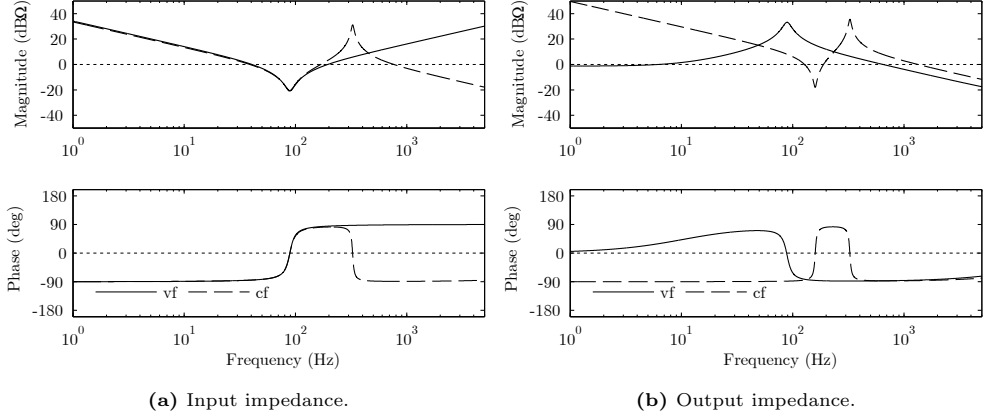


Figure 3.10. Impedance network terminal impedance.

The impedance network will affect the inverter dynamics through its output impedance as shown in (3.72) and (3.76). As the output impedance of the current-fed and voltage-fed model are different, also the dynamics associated with the output current, are different.

The d-component of the control-to-output current transfer function shown in Fig. 3.11a is profoundly affected by the source. The low frequency phase shift of 180° means that an output current control cannot be designed to operate with both sources. Similar tradeoff is not present in q-component of the output current control as shown in Fig. 3.11b.

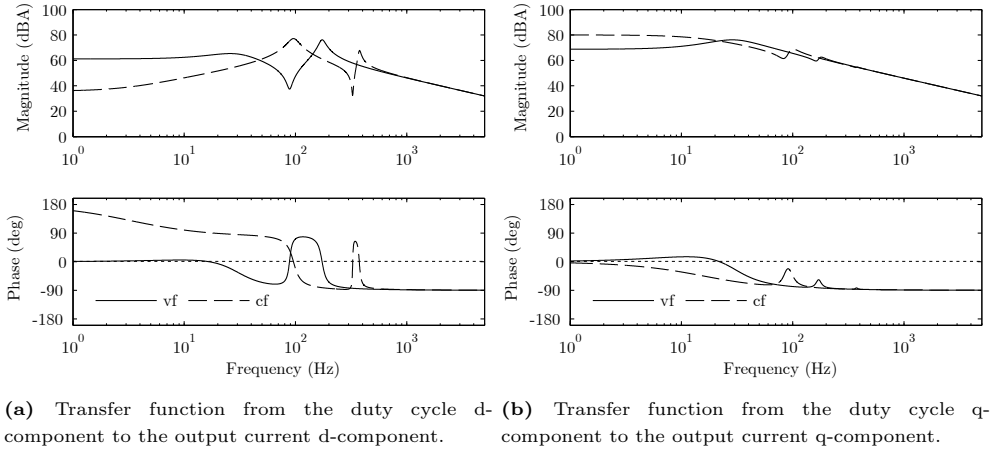
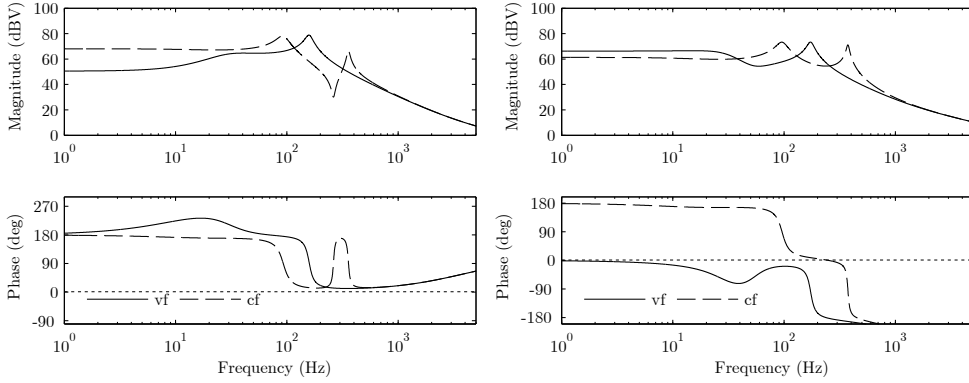


Figure 3.11. Control-to-output transfer functions.

The transfer functions from a shoot-through duty cycle to the impedance network capacitor voltage shown in Fig. 3.12b clearly contains a high-frequency RHP-zero, which can be observed as phase decrease after the frequency of the zero. The same zero is present in the current-fed impedance network. However, the low-frequency phase of the transfer function changes 180° between the models. The transfer function from the d-component of the inverter bridge

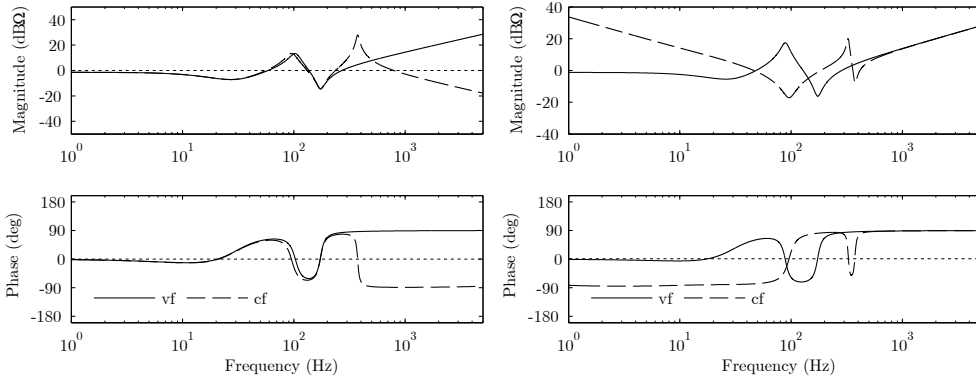
duty ratio shown in 3.12a does not have similar behavior as the transfer function from the shoot-through duty cycle to capacitor voltage.



(a) Transfer function from the duty cycle d to capacitor voltage. (b) Transfer function from shoot-through duty cycle to capacitor voltage.

Figure 3.12. Capacitor voltage related transfer functions.

The Z-source inverter input impedance and the d-component of the output impedance are shown in Figs. 3.13a and 3.13b. The low-frequency behavior of the current-fed model is capacitive compared to resistive behavior of the voltage-fed model. Moreover, as in other transfer functions of the current-fed impedance network, an additional resonant term appears in the input and output impedances.



(a) Input impedance.

(b) D-component of the output impedance.

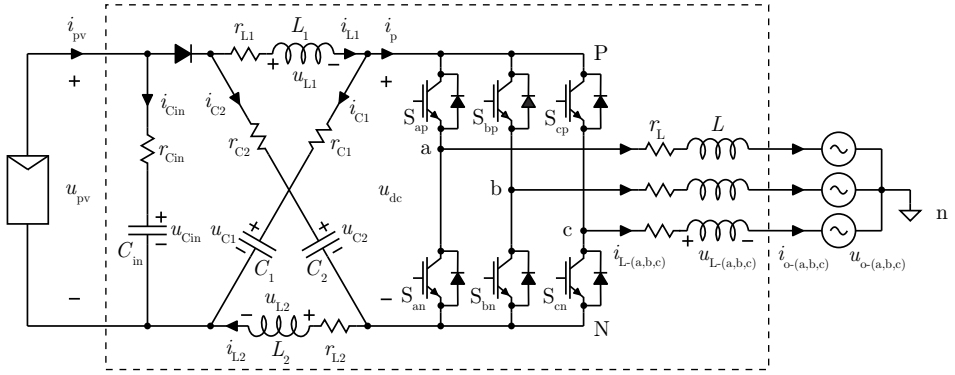
Figure 3.13. Impedance characteristics of a Z-source inverter.

Table 3.1. Z-source inverter parameters used in comparison.

U_{in}	I_{in}	P_{in}	U_{dc}	U_{o-rms}
400 V	25 A	10 kW	700 V	230 V (at 50 Hz)
C_1, C_2	L_1, L_2	C_{in}	L	U_D
500 μ F	1 mH	250 μ F	800 mH	0.7 V
r_{C1}, r_{C2}	r_{L1}, r_{L2}	r_{Cin}	$r_L + r_{sw}$	r_D
10 m Ω	50 m Ω	10 m Ω	100 m Ω	20 m Ω

3.2 Modeling of a photovoltaic Z-source inverter

The model of a photovoltaic Z-source inverter shown in Fig. 3.14, is derived by first computing the effect of the photovoltaic generator on the dynamics of the impedance network. Then it is combined with the model of the VSI-based inverter.

**Figure 3.14.** Three-phase photovoltaic inverter based on conventional ZSI-topology.

Effect of the photovoltaic generator on dynamics of the impedance network

The photovoltaic generator is a highly non-linear source having properties of a voltage source and a current source. To design robust controllers for the interfacing inverter, a method to include the effect of the dual nature of the source is required. The most straightforward method to include the effect is to use the source-affected model of the current-fed impedance network.

The source-affected small-signal characteristics of the current-fed impedance network can be given as

$$\begin{bmatrix} \hat{u}_{pv} \\ \hat{i}_o \end{bmatrix} = \begin{bmatrix} Z_{in}^S & T_{oi}^S & G_{ci}^S \\ G_{io}^S & -Z_o^S & G_{co}^S \end{bmatrix} \begin{bmatrix} \hat{i}_{ph} \\ \hat{u}_{dc} \\ \hat{d} \end{bmatrix}, \quad (3.83)$$

where the source-affected transfer functions denoted by superscript 'S' are

$$Z_{in}^S = \frac{Z_{in}}{1 + Y_{pv} Z_{in}} \quad (3.84a)$$

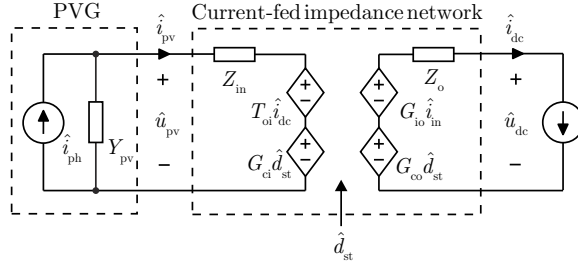


Figure 3.15. Linear model of a current-fed impedance network with non-ideal source.

$$T_{oi}^S = \frac{T_{oi}}{1 + Y_{pv} Z_{in}} \quad (3.84b)$$

$$G_{ci}^S = \frac{G_{ci}}{1 + Y_{pv} Z_{in}} \quad (3.84c)$$

$$G_{io}^S = \frac{G_{io}}{1 + Y_{pv} Z_{in}} \quad (3.84d)$$

$$Z_o^S = \frac{1 + Y_{pv} Z_{in-sco}}{1 + Y_{pv} Z_{in}} Z_o \quad (3.84e)$$

$$G_{co}^S = \frac{1 + Y_{pv} Z_{in-\infty}}{1 + Y_{pv} Z_{in}} G_{co} \quad (3.84f)$$

where

$$Z_{in-sco} = Z_{in} + \frac{T_{oi} G_{io}}{Z_o} \quad \text{and} \quad Z_{in-\infty} = Z_{in} - \frac{G_{io} G_{ci}}{G_{co}}. \quad (3.85)$$

The source-affected impedance-network-capacitor dynamics can be given by

$$\hat{u}_{Cz} = G_{iCz}^S \hat{i}_{ph} + G_{oCz}^S \hat{i}_{dc} + G_{cCz}^S \hat{d}_{st}, \quad (3.86)$$

where

$$G_{iCz}^S = \frac{G_{iCz}}{1 + Z_{in} Y_{pv}} \quad (3.87)$$

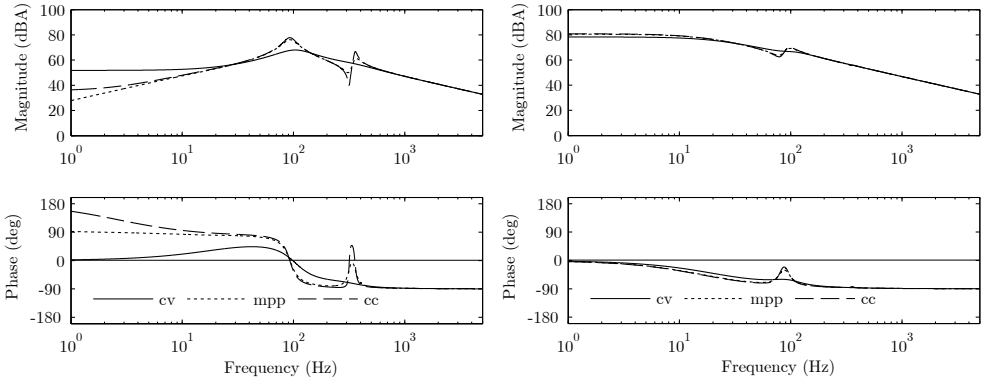
$$G_{oCz}^S = G_{oCz} - \frac{G_{iCz} Y_{pv} T_{oi}}{1 + Z_{in} Y_{pv}} \quad (3.88)$$

$$G_{cCz}^S = G_{cCz} - \frac{G_{iCz} Y_{pv} G_{ci}}{1 + Z_{in} Y_{pv}} \quad (3.89)$$

Effect of the photovoltaic generator on dynamics of the inverter

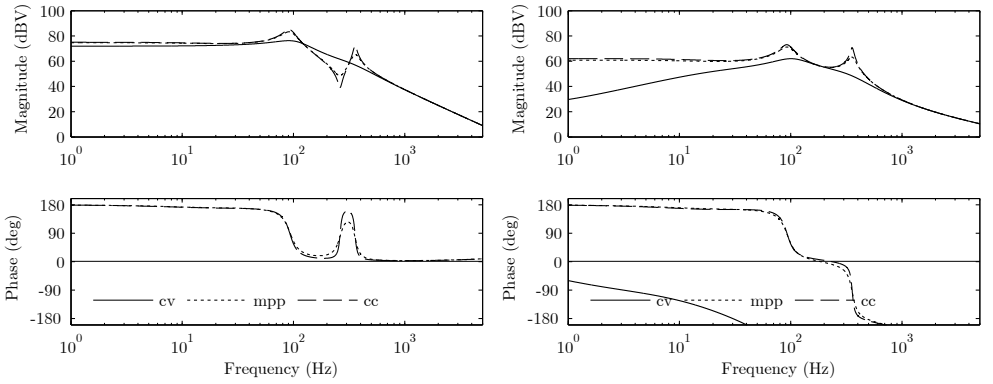
Once the effect of the photovoltaic generator is included in the model of the current-fed impedance network, the complete inverter dynamics can be obtained by using the same modeling method as described in Section 3.1.3 for a real current-fed impedance network.

The d and q-components of the control-to-output transfer function of the photovoltaic Z-source inverter is shown in Figs. 3.16a and 3.16b when the operating point of the PVG is in constant voltage region (cv), constant current region (cc), or at maximum power point (mpp). The response of the system resembles the dynamics of a current-fed network when the operating point of the PVG is in constant-current region, and voltage-fed system when the operating point is in constant voltage region. Similar behavior is visible in the impedance-network-capacitor-voltage-control-related transfer functions shown in 3.17a and 3.17b.



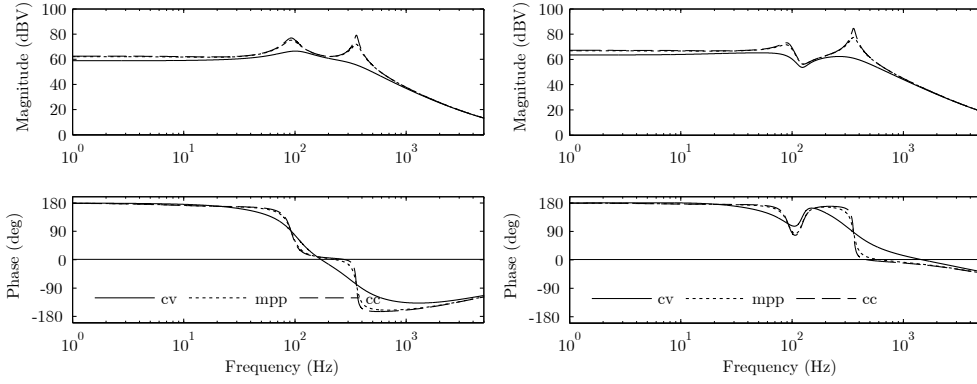
(a) Transfer function from the duty cycle d-component to the output current d-component. (b) Transfer function from the duty cycle q-component to the output current q-component.

Figure 3.16. Control-to-output transfer functions.



(a) Transfer function from the duty cycle d-component to the capacitor voltage. (b) Transfer function from shoot-through duty cycle to capacitor voltage.

Figure 3.17. Capacitor voltage control.



(a) Transfer function from the duty cycle d to the input voltage. (b) Transfer function from shoot-through duty cycle to input voltage.

Figure 3.18. Input voltage control.

The transfer functions related to the input-voltage control are illustrated in Figs. 3.18a and 3.18b. The presented transfer functions imply that the shoot-through duty cycle should be used for input voltage control and the active state control signals to the capacitor voltage control. Due to the profound effect of the photovoltaic generator, it is not feasible to use the shoot-through duty cycle to control the impedance network capacitor voltage.

3.3 Experimental evidence

The validity of the derived small-signal model was evaluated by frequency-domain measurements on a small-scale prototype converter. The space-vector-modulator and the control system of the inverter were implemented using Texas Instruments TMS320F28335 digital signal processor. A solar array simulator manufactured by Agilent was used as a source, and programmable three-phase voltage source Elgar SW5250A as a load. The frequency responses were measured using the frequency response analyzer manufactured by Venable Industries. An overview of the laboratory setup and the prototype converter is presented in Appendix D. The technique used to measure the frequency responses from the prototype converter are discussed e.g. in (Puukko et al.; 2012) and (Jokipii et al.; 2014). Parameters of the emulated solar panel are given in Table 3.2.

Table 3.2. Parameters of the emulated solar array.

U_{pv-mpp}	I_{pv-mpp}	I_{pv-sc}	U_{pv-oc}
25 V	2 A	2.2 A	30 V

Although the inverter operates at open loop, the phase-locked loop (or other equivalent system) must be implemented, since the three-phase grid-connected inverter is unable to operate without proper synchronization to the grid voltage. The open-loop control-related transfer functions are measured in the constant current and constant voltage regions of the

PVG. In the constant-current region, the input voltage equals 23 V, and in the constant voltage-region 27 V, respectively. The impedance network capacitor voltage was set to 35 V in all measurements. The peak value of the three-phase grid phase voltage was 10 V and the frequency 50 Hz. The measurements at open loop are very sensitive to unmodeled characteristics associated e.g. with the PWM and the measurement errors in the custom build hardware, which will explain the differences in the measured and predicted transfer functions.

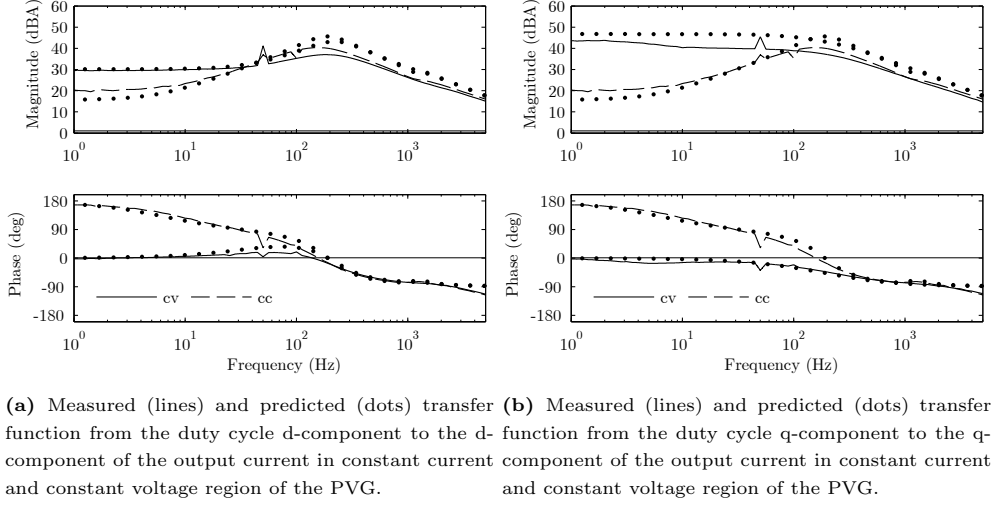


Figure 3.19. Output current control control.

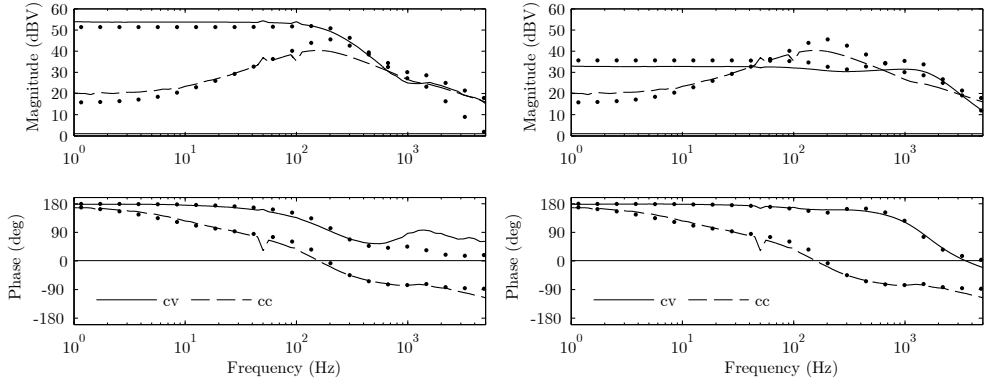


Figure 3.20. Input voltage control and capacitor voltage control.

The measurement results presented in Fig. 3.19a - 3.20b verify the analysis presented in this chapter, thus the proposed small-signal model is suitable for predicting the small-signal characteristics of the photovoltaic inverter for e.g. to design the control loops of the inverter.

3.4 Conclusions

In this chapter, a model for a voltage-fed and a current-fed three-phase grid-connected Z-source inverters was derived. Moreover, using the proposed models it was concluded that the voltage-fed model fails to predict the characteristics of the Z-source inverter when it is supplied from a current source. Thus to represent the dynamics of the Z-source inverter correctly, the system input variables must be selected based on the real application environment. The correct model for a photovoltaic grid-connected Z-source inverter can be constructed by combining the model of a source-affected current-fed impedance network and the model of the VSI-based inverter. The transfer functions presented in this chapter can be used to study the effect of inverter parameters to the shape of the transfer functions and location of the resonances associated to the converter dynamics and design the control loops of the inverter. The derived model also imply that since the source impedance has profound effect of the shoot-through duty cycle to the impedance network capacitor voltage, the shoot-through duty cycle should not be used for capacitor voltage control in photovoltaic applications. Instead, the shoot-through duty cycle should be used for the input-voltage control.

4 ISSUES ON MODELING AND CONTROL OF PHOTOVOLTAIC Z-SOURCE INVERTER

In this chapter, the small-signal model of the Z-source inverter, presented in Chapter 3, is further developed to represent the dynamics of photovoltaic inverter including all control loops. The Z-source inverter is a more complex system than the conventional VSI-based inverter, and some tradeoffs do exist in its control design.

4.1 Impedance network capacitor voltage control

The most simple control scheme for a grid-connected photovoltaic ZSI is illustrated in Fig. 4.1. The fundamental idea is the same as in the dc-link voltage control of the VSI-based inverter: the impedance network capacitor voltage is regulated by adjusting its charge balance by means of the active power exchange with the grid. The reactive power exchange is usually regulated to zero by setting the quadrature component of the output current reference to zero. The maximum power point tracking is implemented by adjusting the shoot-through duty cycle.

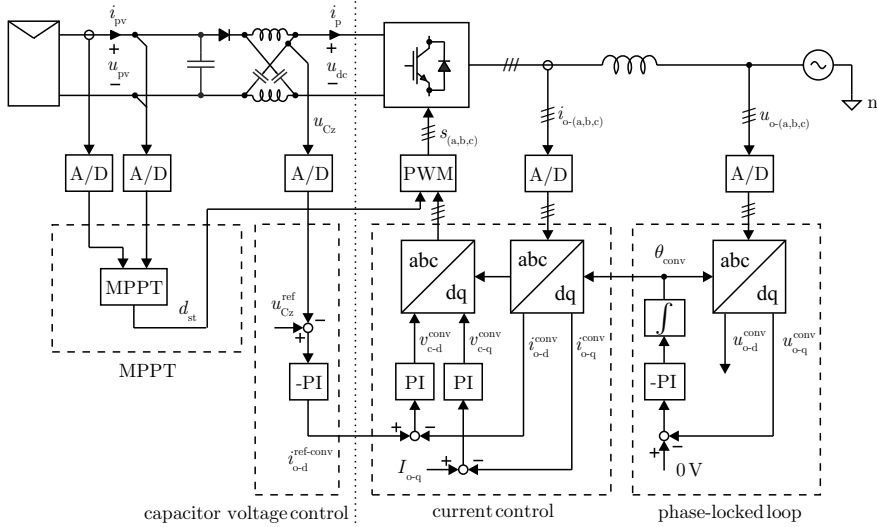


Figure 4.1. Typical synchronous reference frame current control of a maximum-power-point-tracking power converter.

It has been observed that a photovoltaic VSI-based inverter is unstable without the dc-

link-voltage control when the operating point of the PVG is in the constant-current region. The instability is caused by the low-frequency RHP-zero associated to the d-component of the output current control, which becomes a low-frequency rhp-pole when high-bandwidth current control is activated (Puukko and Suntio; 2012). As the high-bandwidth current control is must in a grid-connected inverter, the dc-link-voltage-control loop having the loop crossover frequency higher than the frequency of the pole is required to stabilize the system. Since the circuit structures of photovoltaic VSI and ZSI-based inverters are similar, the same behavior is present also in Z-source inverter. However, since the transfer functions of the system are of fifth order, the system analysis cannot be carried out by using the full-order transfer functions, which is possible in the VSI-based inverter.

The instability can be explained by studying the control block diagram showing the interconnection of the source-affected current-fed impedance network and the output-current-controlled VSI-based inverter illustrated in Fig. 4.2. An internal feedback loop including the output impedance $Z_o^{\text{zn-S}}$ of the source subsystem (the impedance network) and input admittance $Y_{\text{in}}^{\text{vsi-out}}$ of load subsystem (current-controlled VSI-based inverter) is created. As a consequence, every transfer function representing the interconnected system includes the internal feedback loop, e.g. the transfer function from the output-current reference to the dc-link current in the interconnected system can be given by

$$\hat{i}_{\text{dc}} = \frac{1}{1 + Z_o^{\text{zn-S}} Y_{\text{in}}^{\text{vsi-out}}} \mathbf{G}_{\text{ci}}^{\text{vsi-out}} \hat{i}_{\text{o}}^{\text{ref}}. \quad (4.1)$$

According to Middlebrook, the ratio between the source and load impedance as in (4.2) is known as the minor loop gain of a voltage-fed interface. It has been shown that the stability of the interconnected system can be analyzed by studying the minor-loop gain similarly as the loop-gain of a negative feedback control system. As the source and load are stable as standalone systems, the Nyquist criterion can be used to determine the stability. In the simplified version of analysis, the denominator of the loop gain becomes infinite if the source and load impedance are equal and have the phase difference of 180° .

$$L = Z_o^{\text{zn-S}} Y_{\text{in}}^{\text{vsi-out}} = \frac{Z_o^{\text{zn-S}}}{Z_{\text{in}}^{\text{vsi-out}}}. \quad (4.2)$$

Due to the high-bandwidth output-current control, the input terminal of a output current-controlled voltage-fed VSI-based inverter resembles constant power sink inside the current-control bandwidth, i.e., the low-frequency value of the input admittance can be given by:

$$Y_{\text{in-lf}}^{\text{vsi-out}} = -\frac{I_{\text{dc}}}{U_{\text{dc}}} \quad (4.3)$$

The instability thus can take place if the source impedance $Z_o^{\text{zn-S}}$ is higher than $U_{\text{dc}}/I_{\text{dc}}$. When the inverter is fed from a voltage-type source, the source impedance is low and the condition $Z_o < U_{\text{dc}}/I_{\text{dc}}$ is met regardless of the small variations in the output impedance of the source. However, if the source impedance is high at certain frequencies, the instability may take place. According to the model presented in Chapters 3 and 4, in the Z-source inverter, the impedance seen by the inverter bridge is the low-frequency output impedance of the PVG

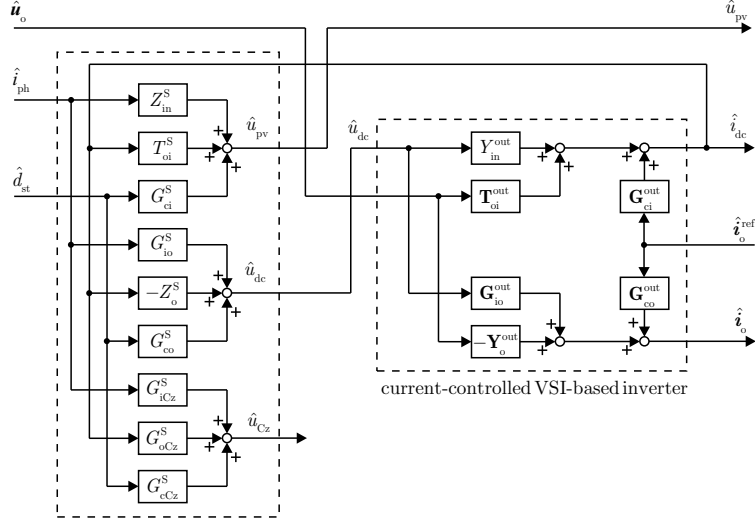


Figure 4.2. Including the effect of non-ideal source on current-controlled VSI-based inverter model.

reflected through the impedance network by the boost-factor, i.e.,

$$Z_{o-lf}^{zn} \approx B^2 r_{pv}, \quad (4.4)$$

where B is the boost-factor.

The origin of the interactions based on the interface impedance are illustrated in Fig. 4.3. The output impedance of a current-type impedance network is capacitive (high impedance at low frequencies), whereas in voltage-fed system the source impedance is naturally small. Thus it is obvious that the interconnection of a real current-fed impedance network and the output-current-controlled VSI becomes unstable. According to (4.4), the most critical point in photovoltaic applications occurs when the impedance network operates at maximum boost factor and the source impedance is high. This is likely to occur at the minimum input voltage. The output impedance and the input impedance are equal when the PVG is operated at the MPP, which means that the interconnected system is marginally stable.

$$Z_{o-lf-mpp}^{zn} \approx B^2 \frac{U_{pv}}{I_{pv}} = \frac{U_{dc}}{I_{dc}}, \quad (4.5)$$

As discussed earlier, the stability of the interconnected system may be analyzed applying the Nyquist criterion on the minor-loop gain. The Nyquist-diagrams for the impedances, shown in Fig. 4.3, are presented in Fig. 4.4. As the impedance network and the output-current-controlled inverter are stable standalone systems, the minor-loop gain does not contain any right-half-plane poles. Thus the criterion for stability is that the minor-loop should not encircle the critical point $(-1,0)$ in the Nyquist diagram. According to Fig. 4.4, the interconnected system becomes unstable when the operating point of the photovoltaic generator moves to the constant-current region.

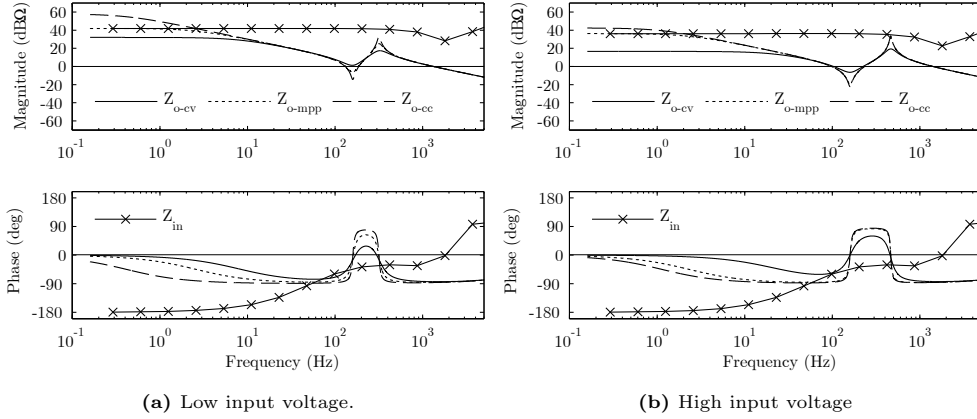


Figure 4.3. Source-affected output impedance of the impedance network.

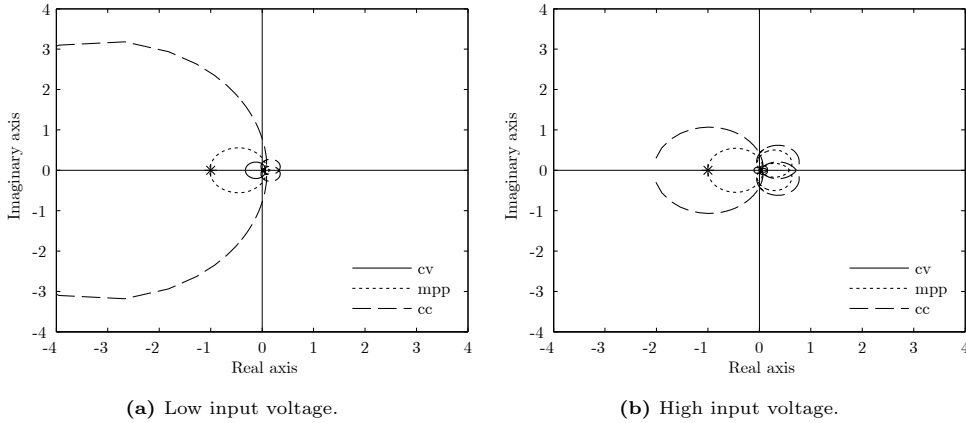


Figure 4.4. Nyquist diagram of the minor loop gain $Z_o^{znS} Y_{in}^{vsi-out}$.

Predicting the frequency of the RHP-pole

Since the photovoltaic inverter must operate in the constant-voltage and constant-current regions of the PVG, the control design must be carried out by taking into account the right-half-plane pole appearing when the current-controlled VSI and the impedance network are interconnected. To design the controller, the frequency, where the interaction takes place, must be known. However, as the output impedance of the impedance network is a high-order transfer function, it is tedious or even impossible to obtain the frequency from the complete transfer function. The low-frequency characteristics can be, however, predicted by using the voltage-fed impedance network model presented in Section 3.1.

The low-frequency equivalent circuit of the voltage-fed impedance network, which is derived based on transfer functions given in (3.32b), (3.32d), and (3.32e), and the photovoltaic generator are shown in Fig. 4.5. The low-frequency behavior of the impedance network forward and reverse transfer functions equal the boost-factor B given in (3.24), and the output

impedance of the network is negligible. The input admittance of the low-frequency model equals the input admittance of the voltage-fed model given in (3.32a).

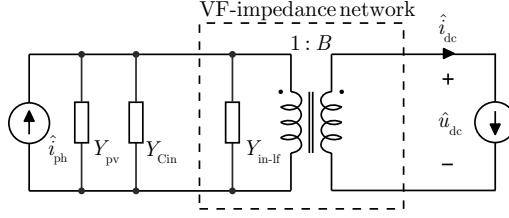


Figure 4.5. Linear circuit used for output impedance approximation.

When a parallel connection of an input capacitor and photovoltaic generator are taken into account, the low-frequency behavior of the impedance network, according to the Fig. 4.5, can be given as

$$Z_{o-lf}^{zn} \approx B^2 Y_{eq}^{-1}, \quad (4.6)$$

where

$$Y_{eq} = Y_{pv} + Y_{in-lf} + Y_{Cin}. \quad (4.7)$$

Inserting the low frequency input admittance of the voltage-fed impedance network (3.32a), admittance of the input capacitor (sC_{in}), and the admittance of the PVG ($1/r_{pv}$) into (4.6) yields

$$Z_{o-lf}^{zn} \approx \frac{B^2 r_{pv}}{s r_{pv} (C_{in} + 2B^2(1 - D_{st})^2 C_1) + 1}. \quad (4.8)$$

The output impedance of the source-affected current-fed impedance network computed by using the full-order model given in Section 3.2 and the approximated output impedance using (4.8) are shown in Fig. 4.6. According to the figure, the approximation predicts the low-frequency characteristics correctly at the different operating points of the PVG.

Finally, when the approximation for the source and load impedance are known, the pole frequency of the interconnected system can be found by solving the characteristic equation

$$1 - \frac{B^2 r_{pv}}{s r_{pv} (C_{in} + 2B^2(1 - D_{st})^2 C_1) + 1} \cdot \frac{I_{dc}}{U_{dc}} = 0. \quad (4.9)$$

The frequency of the pole can be solved from (4.9) yielding

$$\omega_p = \frac{1}{C_{in} + 2 \frac{U_{Cz}^2}{U_{pv}^2} C_1} \left(\frac{I_{pv}}{U_{pv}} - \frac{1}{r_{pv}} \right). \quad (4.10)$$

The pole frequency is positive, i.e. it locates in the right-half of the complex plane, when $r_{pv} > U_{pv}/I_{pv}$. Correspondingly, when $r_{pv} < U_{pv}/I_{pv}$, the pole frequency is negative and it locates in the left-half of the complex plane. The maximum right-half-plane pole frequency can be determined assuming infinite r_{pv} , i.e., a real current-fed inverter. According to (4.10), the maximum RHP frequency can be given as

$$\omega_{p-rhp} = \frac{1}{U_{pv}^2 C_{in} + 2U_{Cz}^2 C_1} P_{pv}. \quad (4.11)$$

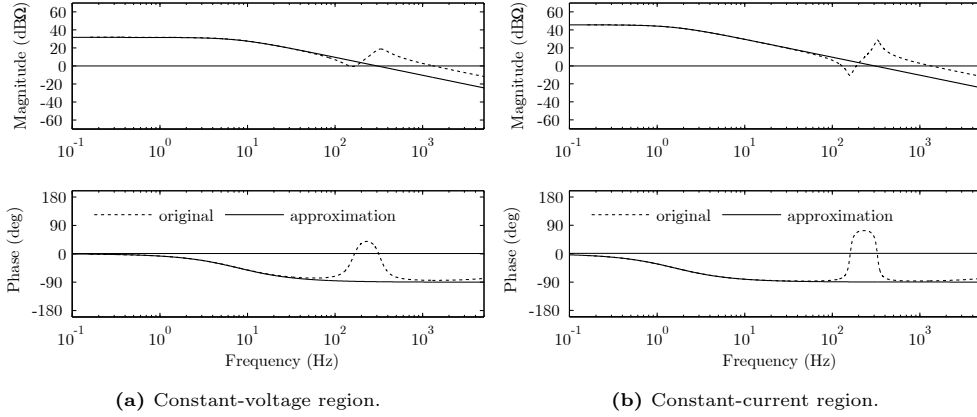


Figure 4.6

At low input voltages, the frequency given by (4.11) is dominated by the second term in the denominator (i.e. $U_{pv}^2 \ll 2U_{Cz}^2$). Thus maximum frequency of the pole can be approximated as

$$\omega_{p-rhp} < \omega_{p-rhp-max} \approx \frac{1}{2U_{Cz}^2 C_1} P_{pv}. \quad (4.12)$$

When the converter operates in buck-mode, the input voltage and the impedance network capacitor voltages are equal. The most critical condition occurs when the voltage gets its minimum value and the current its maximum value, i.e.,

$$\omega_{p-rhp} < \omega_{p-rhp-max} \approx \frac{1}{U_{pv}^2 (C_{in} + 2C_1)} P_{pv} = \frac{I_{pv}}{U_{pv} (C_{in} + 2C_1)} \quad (4.13)$$

Impedance network capacitor voltage control

The impedance-network-capacitor-voltage control is required to maintain the stability of the inverter, since it is required to stabilize the right-half-plane pole caused by the current-type source and grid-current control. The photovoltaic inverter equipped with only output-current control becomes unstable when the operating point moves into the constant current region of the PVG. Fortunately, the feedback from e.g. the capacitor voltage will stabilize the system if the control bandwidth (loop crossover frequency) is higher than the frequency of the unstable pole (Skogestad and Postlethwaite; 2005).

According to Fig. 4.2, the transfer function from output current reference to the equivalent dc-link current can be given by

$$\hat{i}_{dc} = \frac{1}{1 + Z_o^{znS} Y_{in}^{vsi-out}} G_{ci}^{vsi-out} \hat{i}_o^{ref}. \quad (4.14)$$

As only the d-component of the current reference is used in control, (4.14) may be rewritten by

$$\hat{i}_{dc} = \frac{1}{1 + Z_o^{znS} Y_{in}^{vsi-out}} G_{ci-d}^{vsi-out} \hat{i}_{o-d}^{ref} \quad (4.15)$$

Finally, the transfer function from the direct component of the output-current reference to the capacitor-voltage according to Fig. 4.2 can be given by

$$G_{\text{ioCz}} = G_{\text{oCz}}^{\text{znS}} \frac{1}{1 + Y_{\text{in}}^{\text{vsi-out}} Z_{\text{o}}^{\text{znS}}} G_{\text{ci-d}}^{\text{vsi-out}} \hat{i}_{\text{o-d}}^{\text{ref}} \quad (4.16)$$

An example Nyquist diagrams of the loop-gains of a stable and unstable capacitor-voltage-control loop is shown in Fig. 4.7. When the operating point of the PVG is in CC region, the output current controlled system has one unstable pole. The nyquist diagram of the loop gain should thus encircle the critical point once to obtain stable closed-loop system. If the control loop gain is decreased (or the size of the capacitor decreased), the loop gain does not encircle the point and the closed loop system remains unstable.

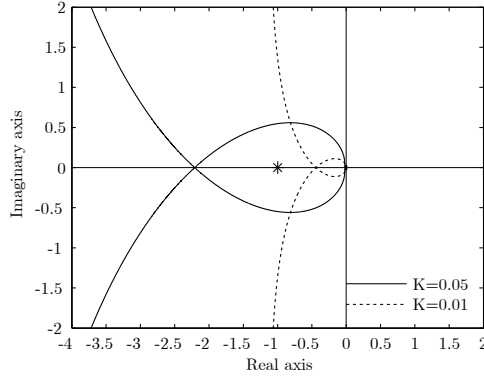


Figure 4.7. Nyquist diagram of the loop gain $G_c^{\text{Cz}} G_{\text{ioCz}}$.

Finally, the closed-loop transfer function including the effect of the capacitor-voltage control is found by substituting the current reference by the output of the impedance network-capacitor-voltage controller similarly as in VSI-based inverter presented in Chapter 2, or alternatively from the control-block diagram shown in Fig. 4.8. The resulting closed-loop transfer functions of the Z-source inverter can be given by

$$\begin{bmatrix} \hat{u}_{\text{pv}} \\ \hat{i}_{\text{o}} \end{bmatrix} = \begin{bmatrix} Z_{\text{in}}^{\text{c}} & \mathbf{T}_{\text{oi}}^{\text{c}} & G_{\text{ri}}^{\text{c}} & G_{\text{sti}}^{\text{c}} \\ \mathbf{G}_{\text{io}}^{\text{c}} & -\mathbf{Y}_{\text{o}}^{\text{c}} & \mathbf{G}_{\text{ro}}^{\text{c}} & \mathbf{G}_{\text{sto}}^{\text{c}} \end{bmatrix} \begin{bmatrix} \hat{i}_{\text{ph}} \\ \hat{\mathbf{u}}_{\text{o}} \\ \hat{u}_{\text{Cz}}^{\text{ref}} \\ \hat{d}_{\text{st}} \end{bmatrix}, \quad (4.17)$$

where

$$Z_{\text{in}}^{\text{c}} = Z_{\text{in}}^{\text{outS}} - G_{\text{ri-d}}^{\text{outS}} \frac{G_{\text{c}}^{\text{uCz}}}{1 + G_{\text{c}}^{\text{uCz}} G_{\text{rCz-d}}^{\text{outS}}} G_{\text{icZ}}^{\text{outS}} \quad (4.18)$$

$$\mathbf{T}_{\text{oi}}^{\text{c}} = \mathbf{T}_{\text{oi}}^{\text{outS}} - G_{\text{ri-d}}^{\text{outS}} \frac{G_{\text{c}}^{\text{uCz}}}{1 + G_{\text{c}}^{\text{uCz}} G_{\text{rCz-d}}^{\text{outS}}} \mathbf{G}_{\text{oCz}}^{\text{outS}} \quad (4.19)$$

$$G_{\text{ri}}^{\text{c}} = \frac{G_{\text{ri-d}}^{\text{outS}} G_{\text{c}}^{\text{rudc}}}{1 + G_{\text{rCz-d}}^{\text{outS}} G_{\text{c}}^{\text{uin}}} \quad (4.20)$$

$$G_{sti}^c = G_{sti}^{outS} - G_{ri-d}^{outS} \frac{G_c^{uCz}}{1 + G_c^{uCz} G_{rCz-d}^{outS}} G_{stCz}^{outS} \quad (4.21)$$

$$G_{io}^c = G_{io}^{outS} - G_{ro-d}^{outS} G_c^{rCz} \frac{1}{1 + G_{rCz-d}^{outS} G_c^{uCd}} G_{iCz}^{outS} \quad (4.22)$$

$$Y_o^c = Y_o^{outS} + G_{ro-d}^{outS} G_c^{uCz} \frac{1}{1 + G_{rCz-d}^{outS} G_c^{uCd}} G_{oCz}^{outS} \quad (4.23)$$

$$G_{ro}^c = G_{ro}^{outS} \frac{G_c^{uCd}}{1 + G_{rCz-d}^{outS} G_c^{uCd}} \quad (4.24)$$

$$G_{sto}^c = G_{sto}^{outS} - G_{ro}^{outS} \frac{G_c^{uCz}}{1 + G_c^{uCz} G_{rCz-d}^{outS}} G_{stCz}^{outS} \quad (4.25)$$

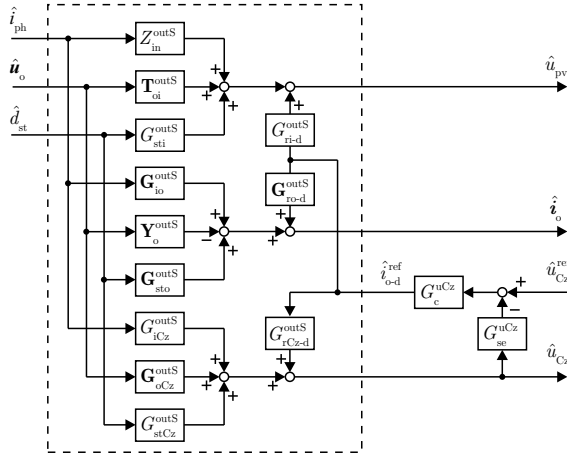


Figure 4.8. Including the effect of non-ideal source on current-controlled Z-source inverter model. The mode inside the dashed equals the model given in Fig. 4.2.

4.2 Determining the value of minimum impedance network capacitance

As discussed in the previous section, the impedance-network-capacitor-voltage control is required to obtain stable closed-loop control system at all operating points of the photovoltaic generator. The crossover frequency of the capacitor voltage-loop must be higher than the pole frequency. According to (Skogestad and Postlethwaite; 2005), the frequency should be twice the unstable pole. In an ideal converter and ideal grid, this can be easily guaranteed. However, in practice it is not feasible to use too high control bandwidth due to the ripple at the frequency of twice the grid frequency caused e.g. by the unbalance in the grid voltages. The control system should be designed to attenuate the ripple generated by the power oscillation, otherwise the grid current will be distorted. As a consequence, the capacitor-voltage-control-loop crossover has to be limited to few tens of hertz. As the frequency of the pole is dictated by the impedance network capacitor voltage and the power of the photovoltaic generator, the

minimum size for the impedance network capacitor can be analyzed as has been previously done for single and two-stage VSI in Messo et al. (2014).

According to the analysis presented in the previous section, the maximum pole frequency in the Z-source inverter equals

$$\omega_{p-\max} \approx \frac{1}{2U_{C_z}^2 C_1} P_{pv} \quad (4.26)$$

When the cloud enhancement (Luoma et al.; 2012) (sudden increase in the power produced by the PVG may increase 1.5 times the nominal power) and the safety margin of two (Skogestad and Postlethwaite; 2005) are considered, a tradeoff between loop crossover frequency, impedance-network-capacitor voltage, and the minimum impedance network capacitance can be formulated as

$$2\pi f_c > 2 \cdot 1.5 \cdot \omega_p \Rightarrow C_1 > \frac{2 \cdot 1.5}{2U_{C_z}^2 2\pi f_c} P_{pv-\text{mpp}}, \quad (4.27)$$

where f_c is the crossover frequency of the impedance-network-capacitor-voltage-control-loop gain. The required capacitance to guarantee stability is illustrated in Fig. 4.9. By using a higher steady state capacitor voltage, a smaller capacitor could be used. However, as a drawback the switching losses will increase. E.g. in 10 kW inverter, where the capacitor voltage is set to 700 V, and the loop-crossover equals 10 Hz, the required capacitance according to (4.27) equals 500 μF .

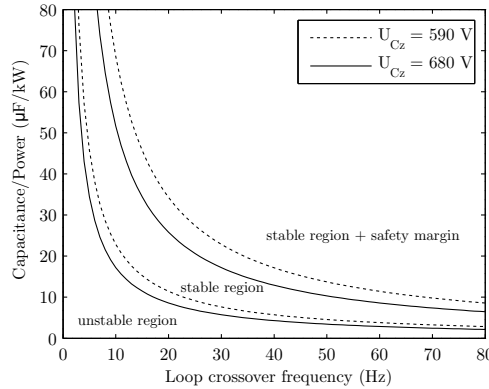


Figure 4.9. Minimum impedance network capacitance requirement for Z-source inverter.

As the pole frequency given by (4.26) does not contain the input capacitance, the input capacitor can be selected to based only on the ripple requirement induced by the PVG.

4.3 Effect of control-mode on control system performance

The impedance network of the Z-source inverter may operate in two modes: i) at open loop as in Section 4.1, or ii) at closed loop as shown in Fig. 4.10, where a feedback loop is added to regulate the input voltage of the converter. The addition of the input-voltage control, as in case of two-stage VSI-based inverter, will improve the MPP tracking performance, and it

is therefore, often utilized. In (Jokipii et al.; 2013), the author have observed that the input voltage control also affects the capacitor-voltage control by removing the right-half-plane pole issue.

The advantage of the input-voltage control can be analytically analyzed by first deriving the model for the input-voltage-controlled-impedance network, and then performing the analysis similar as in section 4.1 was presented for the impedance network operating at open loop.

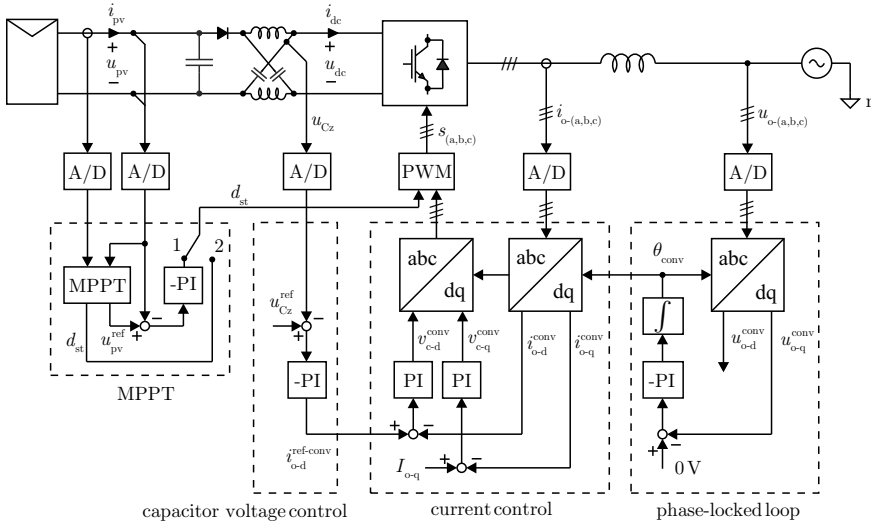


Figure 4.10. Synchronous reference frame current control of a maximum-power-point-tracking Z-source inverter.

Input-voltage-controlled impedance network

When the impedance network is operated at closed loop, the shoot-through duty cycle is adjusted to regulate the input voltage of the converter according to Fig. 4.10. If the sensing gain and the modulator gain are set to unity, the small-signal perturbed shoot-through duty cycle equals:

$$\hat{d}_{st} = G_c^{\text{uin}} \left(\hat{u}_{in}^{\text{ref}} - \hat{u}_{in} \right). \quad (4.28)$$

The transfer function representing the characteristics of the impedance network under input-voltage control may be computed based on the source-affected impedance network model given in Chapter 3 by inserting the perturbed shoot-through duty cycle (4.28) into the open-loop transfer functions and solving the new transfer functions. Alternatively, the closed-loop transfer functions can be solved from the control-block diagram of Fig. 4.11. The closed-loop

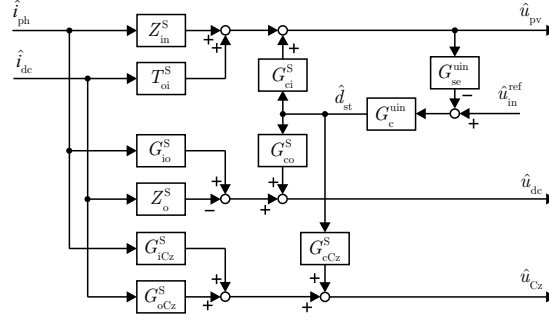


Figure 4.11. Input voltage control of the current-fed impedance network.

model for the impedance network can be given by

$$\begin{bmatrix} \hat{u}_{pv} \\ \hat{i}_o \end{bmatrix} = \begin{bmatrix} Z_{in}^{inS} & T_{oi}^{inS} & G_{ci}^{inS} \\ G_{io}^{inS} & -Z_o^{inS} & G_{co}^{inS} \end{bmatrix} \begin{bmatrix} \hat{i}_{ph} \\ \hat{u}_{dc} \\ \hat{u}_{in}^{ref} \end{bmatrix}, \quad (4.29)$$

where the corresponding transfer functions are

$$Z_{in}^{inS} = \frac{1}{1 + L^{in}} Z_o^S \quad (4.30)$$

$$T_{oi}^{inS} = \frac{1}{1 + L^{in}} T_{oi}^S \quad (4.31)$$

$$G_{ri}^{inS} = \frac{L^{in}}{1 + L^{in}} \quad (4.32)$$

$$G_{io}^{inS} = \frac{1}{1 + L^{in}} G_{io} + \frac{L^{in}}{1 + L^{in}} G_{io-\infty} \quad (4.33)$$

$$Z_o^{inS} = \frac{1}{1 + L^{in}} Z_o^S + \frac{L^{in}}{1 + L^{in}} Z_{o-\infty} \quad (4.34)$$

$$G_{ro}^{inS} = \frac{G_{co}^S}{G_{ci}^S} \frac{L^{in}}{1 + L^{in}}, \quad (4.35)$$

and

$$G_{io-\infty} = G_{io} - \frac{G_{co} Z_{in}}{G_{ci}}, \quad Z_{o-\infty} = Z_o + \frac{G_{co} T_{oi}}{G_{ci}} \quad \text{and} \quad L^{in} = G_{ci}^S G_{pwm} G_c^{uin}. \quad (4.36)$$

In addition, to complete the model, the transfer functions associated to the capacitor can be given by

$$G_{iCz}^{inS} = G_{iCz}^S - G_{cCz}^S \frac{G_c^{in}}{1 + L^{in}} Z_{in}^S \quad (4.37)$$

$$G_{oCz}^{inS} = G_{oCz}^S - G_{cCz}^S \frac{G_c^{in}}{1 + L^{in}} T_{oi}^S \quad (4.38)$$

$$G_{rCz}^{inS} = \frac{G_c^{uin}}{1 + L^{in}} G_{cCz}^S \quad (4.39)$$

According to the given closed-loop transfer functions, under the input-voltage control, the low-frequency behavior of the impedance-network output impedance resembles constant power source, i.e. $Z_{o-\infty}$, regardless of the source impedance. As a result, the impedance-based interaction described in previous section takes place at dc (i.e. zero frequency) and the pole of the interconnected system is thus located in the origin. As a result, there is no requirement for the bandwidth of the capacitor voltage control or minimum size for the impedance network capacitor value. For comparison, the output impedance of the impedance network operating at closed loop is shown in Fig. 4.12. When the impedance network operates at closed loop, the magnitude of the output impedance at low-frequencies is equal to the input impedance of the output-current-controlled VSI-based inverter.

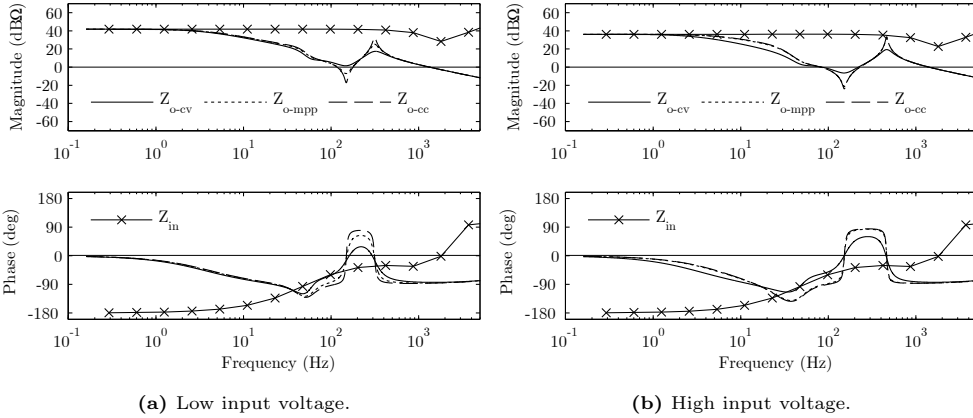


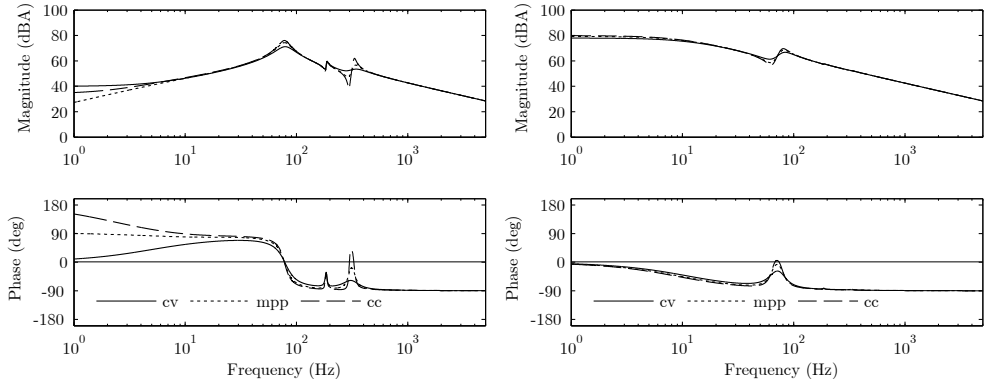
Figure 4.12. Source-affected output impedance of the impedance network when the input voltage control is active.

4.4 Effect of asymmetric impedance network on control system performance

The impedance network passive component parameters may have small mismatch, i.e. $L_1 \neq L_2$, $C_1 \neq C_2$ or both, and the impedance network becomes asymmetric. In symmetric impedance network, the original system order five (five memory elements) is reduced to three due to the pole-zero cancellation. In asymmetric network, the cancellation does not occur and additional dynamics are introduced. In (Jokipii and Suntio; 2015), the author studied the effect of mismatch by comparing the frequency responses from the symmetric and asymmetric impedance network.

As the model presented in Chapter 3 is the full order model, the same model can be utilized to include the effect of asymmetric impedance network as well. The mismatch will create complex pole pair, which is damped only by the equivalent series resistances of the inductors and capacitors, which are often very small. The effect of the asymmetric impedance network

to the current control design can be studied by analyzing the control-to-output transfer shown in Figs. 4.13a and 4.13b. The inverter parameters are the same as in the model presented in Chapter 3 with the exception that $L_2 = 1.5 \cdot L_1$ and $C_2 = 1.5 \cdot C_1$. Comparing responses to those presented in Chapter 3 (Figs. 3.16a and 3.16b), an additional resonance appears between the original resonances. However, the effect is negligible even if the studied model has relatively small parasitic resistances and very large mismatch between the component values. Thus it can be concluded that the asymmetric impedance network does not affect the current control design.

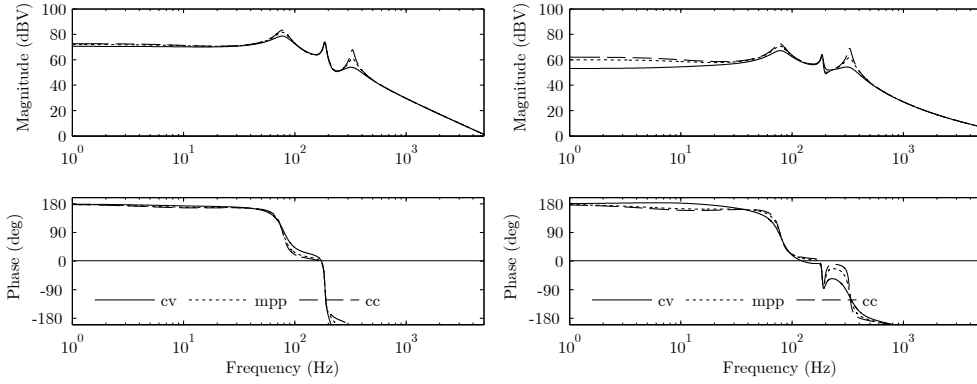


(a) Transfer function from the duty cycle d- (b) Transfer function from the duty cycle q- component to the output current d-component. component to the output current q-component.

Figure 4.13. Control-to-output transfer functions.

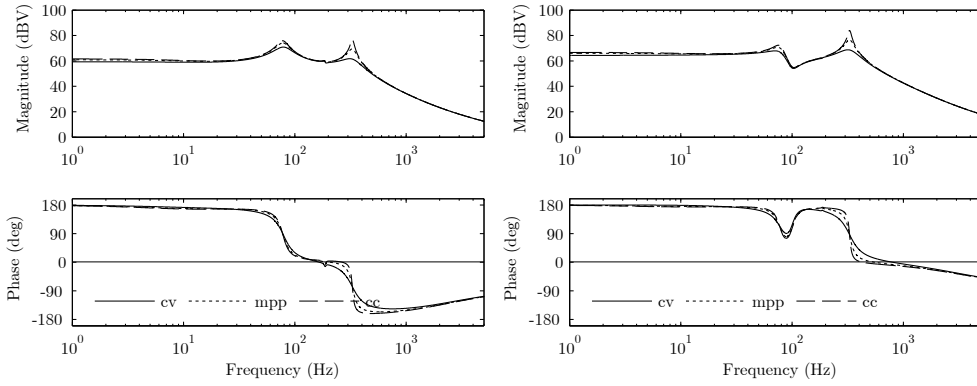
The effect of the asymmetric impedance network to the capacitor-voltage-control design can be studied by analyzing the capacitor-voltage control related transfer functions shown in Figs. 4.14a and 4.14b. The mismatch will decrease the achievable bandwidth of the capacitor voltage control. But since in the grid-connected applications the capacitor-voltage-control loop is designed to obtain bandwidth only up to few tens of hertz, the phase drop does not affect the control design. However, the mismatch in the impedance network components significantly decreases the achievable control bandwidth, if the shoot-through duty cycle is used to regulate the capacitor voltage with a large bandwidth. The reason is the decrease in the phase behavior of the shoot-through duty-cycle to the capacitor-voltage transfer function shown in Fig. 4.14b, which does not appear in the symmetric impedance network. Similar conclusions for the capacitor voltage control in voltage-fed ZSI have been presented e.g. in (Upadhyay et al.; 2011).

Finally, the effect of the asymmetric impedance network to the input-voltage control design is studied by analyzing the input-voltage-control-related transfer functions shown in Figs. 4.15a and 4.15b. According to Fig. 4.15b, the recommended control scheme, where the shoot-through duty is adjusted to regulate the input voltage, is not affected by the impedance network asymmetry.



(a) Transfer function from the duty cycle d to the capacitor voltage. (b) Transfer function from shoot-through duty cycle to capacitor voltage.

Figure 4.14. Capacitor voltage control.



(a) Transfer function from the duty cycle d to the input voltage. (b) Transfer function from shoot-through duty cycle to input voltage.

Figure 4.15. Input voltage control.

4.5 Experimental evidence

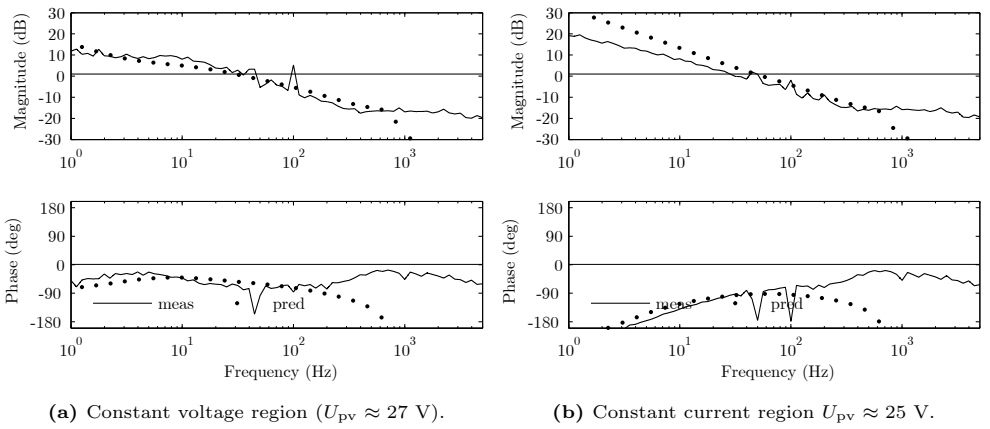
The validity of the derived small-signal model was evaluated by frequency-domain measurements on a small-scale prototype converter. The space-vector-modulator and the control system of the inverter were implemented using Texas Instruments TMS320F23358 digital signal processor. A solar array simulator manufactured by Agilent was used as an input source, and programmable three-phase voltage source Elgar SW5250 as a load. The frequency responses were measured by using the frequency response analyzer manufactured by Venable Industries. An overview of the laboratory setup and the prototype converter is presented in Appendix D. Parameters of the emulated solar panel are given in Table 4.1.

Table 4.1. Parameters of the emulated solar array.

U_{pv-mpp}	I_{pv-mpp}	I_{pv-sc}	U_{pv-oc}
25 V	2 A	2.2 A	30 V

Right-half-plane zero in the control dynamics and input voltage control

To verify the impedance-network-capacitor-control related issues, the loop-gain of the of the capacitor-voltage loop was measured. The measurement results are shown in Figs. 4.16b and 4.16a, which verify that the proposed model can approximate the control-loop bandwidth quite accurately. The measurements are not valid at high frequencies due to lack of resolution in the measurement setup.

**Figure 4.16.** Measured loop-gain of the capacitor voltage control.

As the loop-crossover frequency is higher than the maximum right-half-plane zero, the control system should be stable at all operating points of the photovoltaic generator. Fig. 4.17a shows the measured system response when the shoot-through duty ratio is varied to adjust the input voltage. The control systems is stable at all operating points. The relationship between the shoot-through duty cycle and the input voltage is not linear, thus the slope in the input voltage is not linear.

However, when the capacitor-voltage control bandwidth is decreased, the system stability is compromised when the operating point is in the constant current region as Fig. 4.17b clearly shows. Adding the input-voltage controller will remove this limitation, and the system is stable even with a relatively slow impedance-network-capacitor-voltage controller. The response of the system when the impedance network operates at closed loop is shown in Fig. 4.17c, which verifies the analysis.

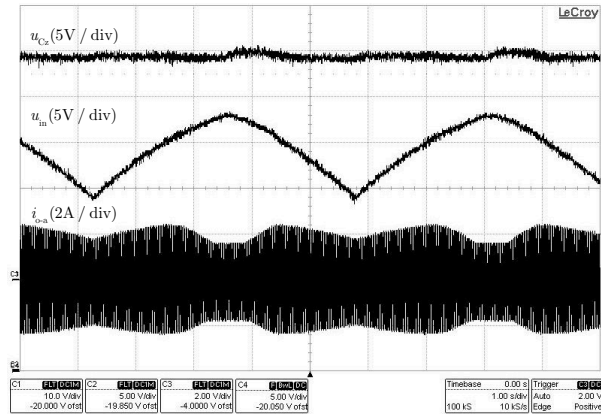
Asymmetric impedance network

To study the effect of asymmetric impedance network, the parameters of the prototype impedance network are modified so that $L_1 = 200 \mu\text{H}$ and $L_1 = 150 \mu\text{H}$. The measured

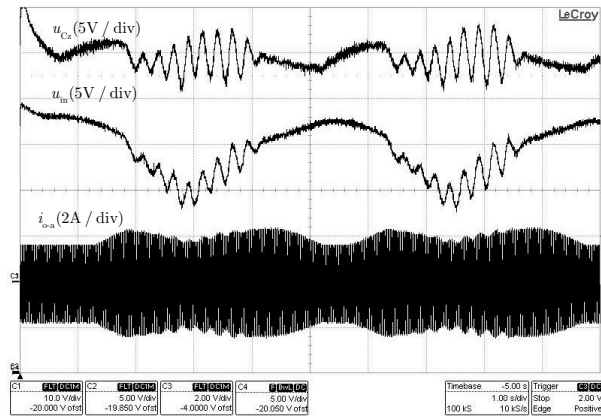
frequency responses of the system are identical to those presented in Chapter 3 and are not repeated here. The time-domain measurement, presented in Figs. 4.18a and 4.18b, indicate that the asymmetric impedance network does not affect the response of the system. Measurements are carried out in the current region of the PVG, since the damping of the system is lowest in when the PVG dynamic resistance is high. The transient response with the asymmetric impedance network do not contain any additional oscillation. Moreover, the measured output impedance presented in Figs. 4.19a and 4.19b, verifies the accuracy of the closed-loop model with the control loops and the asymmetric impedance network.

4.6 Conclusions

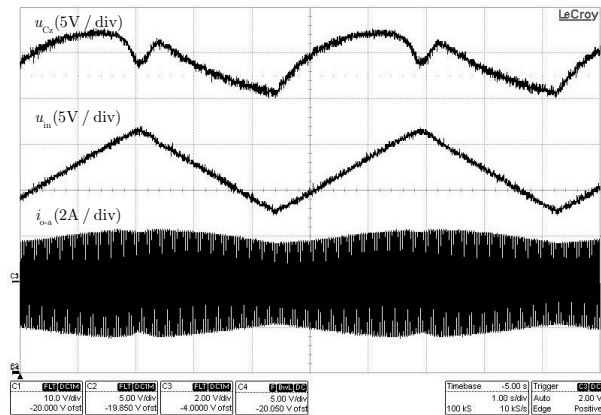
This chapter discussed the control design of a grid-connected photovoltaic Z-source inverter. According to the presented analysis, the control of the inverter should be based on regulating the input voltage by using the shoot-through duty cycle, and the impedance-network-capacitor-voltage control should be implemented by using the conventional cascade control, where the high bandwidth current forms the innermost loop. To improve the dynamic performance, the input voltage of the converter should be regulated by adjusting the shoot-through duty cycle. The validity of the analysis was verified by means of laboratory measurements. It was shown that the proposed model can predict the loop gain of the capacitor-voltage-control loop and if the control bandwidth is decreased the instability associated with the right-half-plane zero will cause undesired oscillations. In addition, the measurements carried out with the inverter equipped with an asymmetric impedance network verify that the mismatches in the impedance network parameters do not compromise the stability of the system or affect the transient response.



(a) Input voltage sweep when the impedance network operates in open-loop and the control design satisfies the design criteria given.

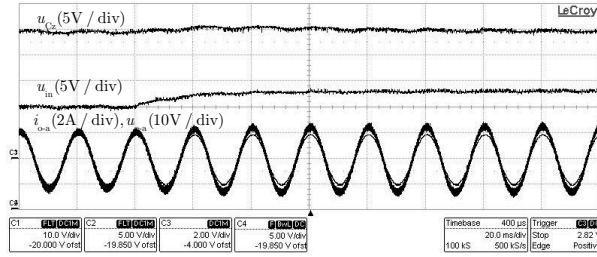


(b) Input voltage sweep when the impedance network operates in open-loop and the control design does not satisfy the design criteria given.

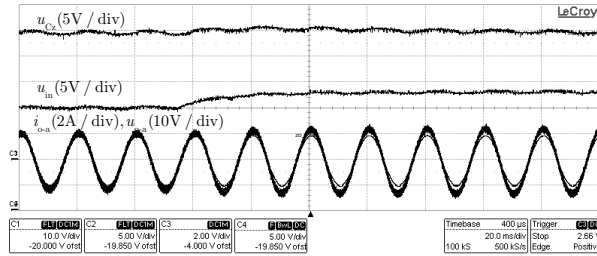


(c) Input voltage sweep when the impedance network operates in closed-loop. Same impedance network capacitor voltage controller as in Fig. 4.17b is used.

Figure 4.17. Input voltage sweep.

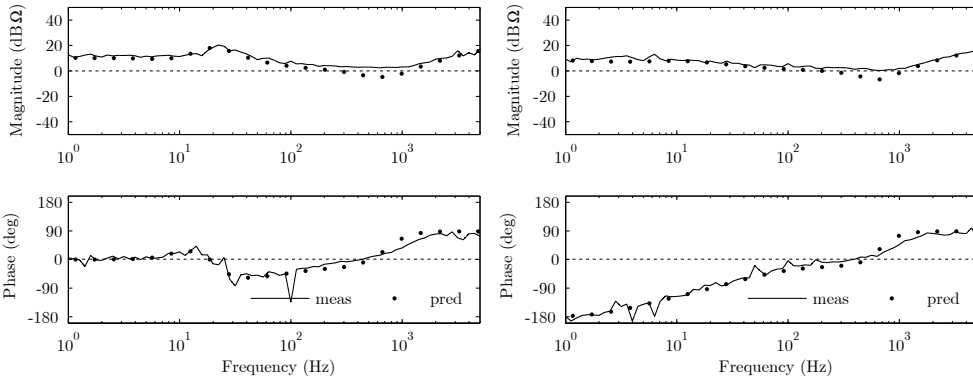


(a) Symmetric impedance network.



(b) Asymmetric impedance network.

Figure 4.18. System response when 3 V step is applied to input voltage reference.



(a) Direct component.

(b) Quadrature component.

Figure 4.19. Measured output impedance of the Z-source converter equipped with asymmetric impedance network.

5 COMPARISON OF DYNAMIC CHARACTERISTICS OF VSI AND ZSI-BASED PV INVERTERS

In this chapter, the similarities and differences between the dynamic properties of ZSI and VSI-based inverter are discussed. The comparison is carried out by utilizing the small-signal models presented in the previous chapters of this thesis.

5.1 Appearance of RHP zero in dynamics

Current-fed single and two-stage VSI-based inverters and the current-fed Z-source inverter incorporates a low-frequency right-half-plane zero in the control related transfer functions. The zero must be taken into account in the control design and it determines also the minimum size for the capacitor in the dc-link of the VSI-based inverter or impedance network capacitor in Z-source inverter.

In grid-connected applications, the minimum dc-link voltage of a VSI-based inverter and the minimum impedance network capacitor voltage of a Z-source inverter are dictated by the grid voltage. The voltage at the dc-side of the inverter-bridge must be higher than the peak value of the line voltage with a sufficient margin. In the two-stage VSI-based inverter and Z-source inverter, the inverter input voltage, i.e. the PVG voltage, can be regulated to a lower value than this limit by utilizing the two-stage inverter boost-stage or Z-source impedance network.

Voltage-boost mode

When the boost stage of the current-fed two-stage VSI-based inverter is operated at open loop, the right-half plane zero associated to the control dynamics can be given as (Messo et al.; 2014):

$$\omega_{\text{rhp}} \approx \frac{P_{\text{pv}}}{C_{\text{dc}} U_{\text{dc}}^2} \quad (5.1)$$

According to results presented in Chapter 4, the right-half plane zero of the current-fed Z-source inverter can be given as:

$$\omega_{\text{rhp}} \approx \frac{P_{\text{pv}}}{C_{\text{in}} U_{\text{pv}}^2 + 2C_1 U_{\text{Cz}}^2} \quad (5.2)$$

However, as discussed in Chapter 4, the input capacitor has very small contribution to the maximum zero frequency when the input voltage is low, since $U_{\text{pv}}^2 \ll 2U_{\text{Cz}}^2$, which indicates

that

$$\omega_{\text{rhp}} \approx \frac{P_{\text{pv}}}{2C_1 U_{\text{Cz}}^2} \quad (5.3)$$

According to (5.1) and (5.3), the RHP-zero frequencies of the two-stage VSI and the ZSI are the same if the same amount of capacitance is connected to the dc-link or in the impedance network. Thus the small-signal stability of the Z-source inverter can be guaranteed by using the same equation with the exception that both impedance network capacitors contributes. The most critical condition occurs at the maximum power point.

When the aforementioned inverters are operated at closed loop, i.e., under input voltage control, the zero moves from right-half-plane to origin. As a consequence, there are then no requirements for the dc-link voltage control or the impedance network capacitor voltage control to stabilize the system.

Voltage-buck mode

In VSI-based single-stage inverter operating in buck mode, the frequency of the zero equals

$$\omega_{\text{rhp}} = \frac{I_{\text{dc}}}{C_{\text{dc}} U_{\text{dc}}} \quad (5.4)$$

When the two-stage inverter is operated in the buck-mode and the boost stage is shorted or its duty ratio is set to zero, the capacitors associated to the boost converter increases the equivalent capacitance connected to the dc-link. Accordingly, when the Z-source inverter is operated in the buck-mode, i.e. when the boost stage is shorted or its duty ratio is set to zero, the capacitors associated with the boost converter increases the equivalent capacitance connected to the dc-link. The maximum limit given by the (5.4) is sufficient to guarantee small-signal stability. The most critical condition occurs at minimum input voltage and maximum input current.

5.2 Output impedance

The interaction of the grid-connected inverter and the utility grid can be analyzed by using the output impedance of the inverter. As the inverter stage and the grid-current control scheme of the Z-source inverter and the single and two-stage VSI-based inverters are similar, it is quite natural that the output impedance of the Z-source inverter resembles the output impedance of the VSI-based inverter. (Jokipii et al.; 2014) (Messo et al.; 2013)

The actual shape of the output impedance of the VSI-based inverter including all the control loops can be predicted by using the model presented in Chapter 2. An example of the single-stage-inverter output impedance operated at open loop is presented in Fig. 5.1. The shape of the impedance is similar to the output impedance of the Z-source inverter shown in Fig. 5.2, which can be predicted by using the model presented in Chapter 4.

The additional high-frequency resonance in Figs. 5.1 - 5.1 originates from the impedance network characteristics. When the impedance network is operated at open loop, the series resonance associated to the impedance network affects the current control of the inverter. The

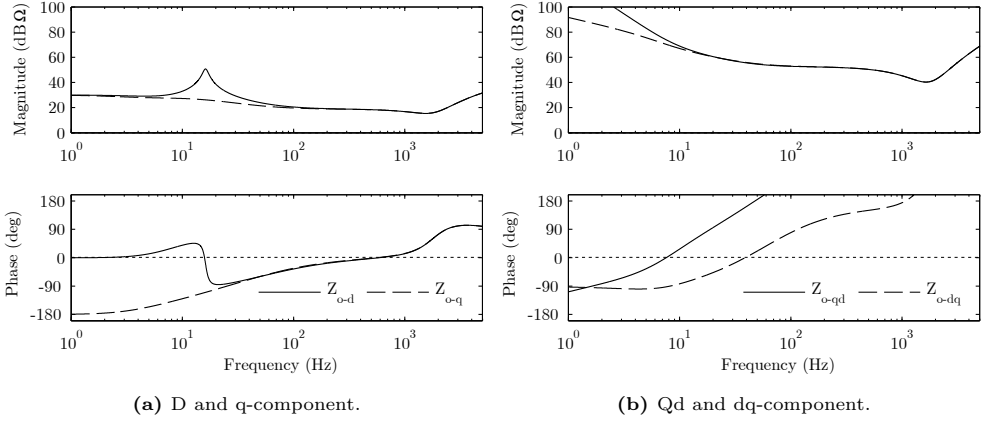


Figure 5.1. Output impedance of a VSI-based single-stage inverter.

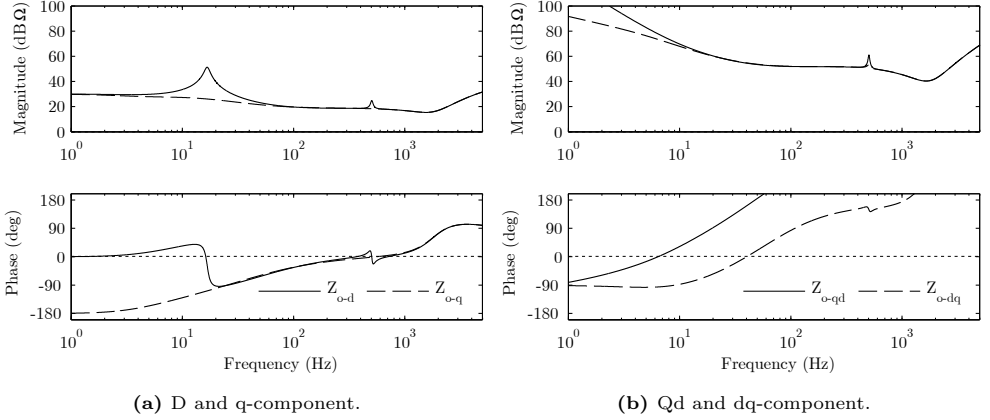


Figure 5.2. Output impedance of a Z-source inverter when the impedance network is operated at open loop.

low-bandwidth voltage controller does not affect the high-frequency behavior of the output impedance. When the impedance network is operated at closed loop, the resonance originates from the voltage control, as the resonance is also visible in the output current-to-capacitor transfer function. With an input voltage control and capacitor voltage control having enough attenuation at the resonance frequency, the additional resonance can be attenuated. However, as the magnitude of the resonance is insignificant, there is basically no difference in the output impedance.

Based on the provided model, the shape of the output impedance is similar to those of VSI-based inverter and does not contain additional magnitude or phase drops that might compromise the stability of the inverter in interconnected system. The main issues regarding the stability are thus the same as in VSI based inverter, i.e. such as the delay in the control loop and the grid-synchronization and can be analyzed in a similar way as in VSI-based

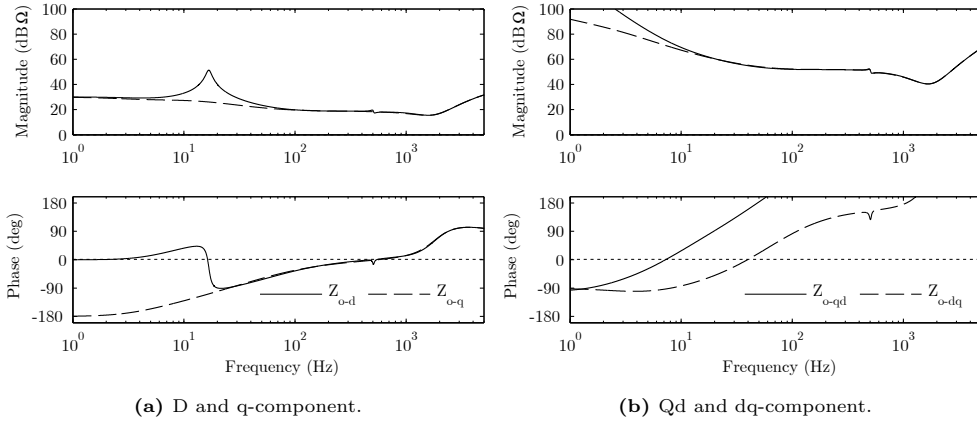


Figure 5.3. Output impedance of a Z-source inverter when the impedance network is operated at closed loop.

inverter. (Messo et al.; 2013) (Harnefors et al.; 2015)

5.3 Input voltage control

As discussed in the previous chapters, the two-stage VSI-based inverter and the Z-source can be equipped with an input-voltage controller. Moreover it was concluded that the input-voltage control is the recommended control mode of the inverter. The system settling time in the closed-loop operation is mainly dictated by the bandwidth of the control loops, the natural resonance frequency of the system, and the damping of the system. When the input voltage is regulated by the feedback control, the MPPT-facility operates at closed loop, where the tracker gives the reference for the input voltage control.

Design of the input voltage control

The design and performance of the input voltage control can be compared by analyzing the control-to-input transfer function of the conventional boost-stage and the impedance network present in the Z-source inverter. In both converters, the transfer function has a resonant frequency that depends on the parameters of the passive components. Moreover, in Z-source inverter also the operating point affects the location of the resonance. The dynamic resistance of the PVG does not affect the location of the resonance but affects the system damping.

According to the small-signal model presented in Chapter 3. The resonant frequency of the impedance network is lowest and the damping is low when the input voltage and the PVG dynamic resistance are low. This condition is unlikely to happen but is possible e.g. in partial shading conditions when the global maximum-power point exists at the low voltages (see Chapter 1, Fig. 1.6).

Since the shape of the control-to-input transfer functions of the boost-power-stage and the Z-source inverter are similar, the same control tuning methods can be utilized. When

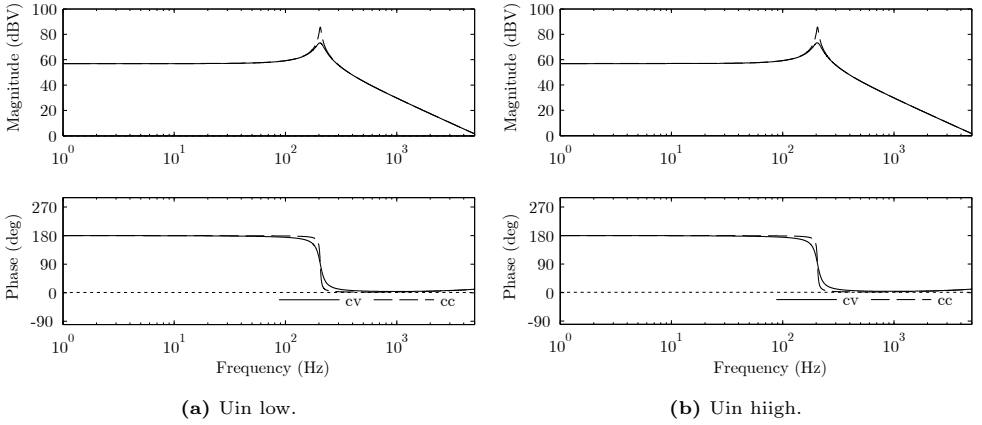


Figure 5.4. Control-to-input transfer function of boost converter.

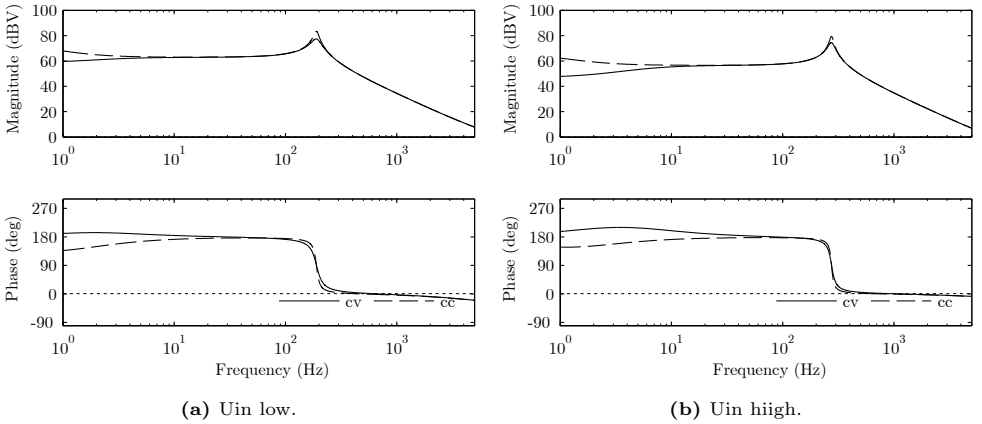


Figure 5.5. Control-to-input transfer function of Z-source inverter impedance network.

the control-loop is designed based on the low-input voltage, the bandwidth slightly increases when the input voltage is increased. A conventional PI-type controller is sufficient to drive the system into the correct steady state. A more complex PID-type controller is required to obtain bandwidth over the resonance. As a consequence of the similar control-to-input transfer functions, the closed-loop system representing the ability to track the input voltage reference, are also similar. The input voltage reference tracking of the Z-source inverter can be designed to be similar as in VSI-based two-stage inverter.

However, in two-stage inverter, the input voltage loop-crossover frequency can be chosen to be very high. This is not feasible in ZSI, since the input capacitor is a part of the equivalent dc-link voltage and thus if the control bandwidth is higher than the output current control, the output current of the inverter becomes distorted when the input voltage reference or the input current is perturbed. A constant perturbation is required in MPP-tracking converter would vary accordingly. In two-stage inverter, the large dc-link capacitor acts as a power

buffer and similar behavior does not take place. The main drawback of the Z-source inverter in comparison to the two-stage inverter is thus the requirement for the location of the system resonance. The resonance should be limited to lower than the output current control bandwidth with a sufficient margin.

5.4 Conclusions

The dynamics of the VSI-based inverters and the Z-source inverter contains a low frequency right-half-plane zero in the control-related transfer functions. The zero must be taken into account in the dc-link voltage control and in the impedance-network-capacitor-voltage control. It was shown that the design rule previously derived for selection of the two-stage VSI-based inverter dc-link capacitance can be also utilized in Z-source inverter. In addition, it was shown that the input-voltage control design can be carried out in a similar way as in the two-stage VSI-based inverter and the similar control performance can be obtained. Finally, it was shown that the shape of the output impedance of the Z-source inverter and the VSI-based inverter are similar.

6 CONCLUSIONS

6.1 Final conclusions

As concluded by several research groups, the three-phase Z-source inverter is suitable for interfacing of a photovoltaic power generator into the utility grid. However, the dynamic characteristics of the converter is often analyzed without taking into account the effect of the real source behavior, which may hide important details about the system stability and performance under varying operating conditions such as in the photovoltaic applications where the PV-generator impedance varies according to the operating point. This thesis presented an accurate modeling method to evaluate the dynamic characteristics of the Z-source inverter, discussed the issues related to the control of the inverter, and finally compared several characteristics of the Z-source inverter to those of the conventional VSI-based inverter. In terms of dynamic characteristics, there seem to be no major disadvantages (or advantages) in ZSI over the traditional photovoltaic inverter.

In Chapters 2 and 3, a consistent method to model the dynamic characteristics of the three-phase grid-connected Z-source inverter was presented. The analysis was carried out by developing an accurate small-signal model for the inverter, which was used to highlight the differences between the dynamics of a voltage-fed and a current-fed Z-source inverter and further developed to model the photovoltaic inverter. The voltage-fed model was shown to present the characteristics of a photovoltaic inverter incorrectly. Thus to capture the dynamics correctly and to include all the control loops, the photovoltaic Z-source should be analyzed as a current-fed system and the effect of the photovoltaic generator was included by using the proposed source-affected model.

According to Chapter 4, the control of the photovoltaic Z-source inverter should be based on regulating the input voltage of the converter by adjusting the length of the shoot-through state, and the impedance network capacitor voltage control should be implemented using cascade controlled output current control, where the slow capacitor-voltage control adjusts the reference of the fast output current control. When the converter operates under feedback from the input voltage, the right-half-plane zero associated to the output-current control disappears. Without the input voltage control, the stability of the inverter may be compromised. In addition, it was shown in Chapter 4 that the small mismatch in the impedance network parameters causes additional resonances in the system but does not compromise the stability and performance of the inverter.

In Chapter 5, the characteristics of a Z-source inverter was compared to VSI based inverter.

The previously published method to determine the minimum capacitance required in the dc-link of the two-stage inverter was shown to be similar to the limit proposed for the Z-source inverter in Chapter 4. The output impedance of a Z-source inverter resembles the output impedance of a conventional inverters. In addition, the input-voltage-control bandwidth can be designed to be similar as in two-stage VSI-based inverter, which provides a sufficient maximum-power-point tracking performance.

6.2 Future topics

The author's recommendations for the future topics regarding the research of a Z-source inverter include:

- The output current control bandwidth varies as a function of the equivalent dc-link voltage. As a result, the output current control performance and thus the shape of the output impedance varies as a function of the input voltage of the inverter. In ideal case, the current control is not affected by the voltage level. The effect of gain scheduling together, which is usually indirectly included by using the space-vector pulse-width modulation, effect should be studied.
- The impedance network of the Z-source inverter contains reactive elements and an oscillating energy transfer will occur between the components in certain conditions. The phenomenon is amplified if there is mismatch in the impedance network parameters. In this work, a high-bandwidth-input-voltage control can be used to damp the oscillation. A need for more sophisticated damping (e.g. current control in impedance network) should be studied.
- The impedance network inductor can be wound on the same core. The effect of the coupling on the dynamics should be included in the model.
- Main differences between the dynamic-characteristics of quazi-ZSI and other derived topologies, should be studied.
- In this thesis, only MPPT operation was discussed. However, the converter may operate also in the power limiting mode, i.e., when the voltage-control current reference is saturated. This is a natural result of a downsized inverter. This is actually a property of a MPP-tracking converter also, since it is very customary to downsize the inverter in respect to the PVG power. The inverter operating in power limiting mode basically has only current control. Inverter works fine if the PVG operating point of the inverter is in voltage region but becomes unstable when the operating point moves to the current region.

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A ALPHA-BETA AND DIRECT-QUADRATURE -FRAMES

Alpha-beta -frame representation of three-phase signals

The amplitude invariant abc-to- $\alpha\beta 0$ -frame transformation, also known as the Clarke transformation, and its inverse transformation are defined as

$$\begin{bmatrix} x_\alpha \\ x_\beta \\ x_0 \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} \quad (\text{A.1})$$

and

$$\begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} = \begin{bmatrix} 1 & 0 & 1 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} & 1 \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} & 1 \end{bmatrix} \begin{bmatrix} x_\alpha \\ x_\beta \\ x_0 \end{bmatrix}. \quad (\text{A.2})$$

In three-phase systems without the neutral conductor (as in the inverter circuits analyzed in this thesis), the zero-sequence circuit is open-circuited and as a result the zero-sequence current cannot flow. To simplify the analysis, the zero-sequence is neglected and the transformations used in this thesis are

$$\begin{bmatrix} x_\alpha \\ x_\beta \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} \quad (\text{A.3})$$

and

$$\begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} x_\alpha \\ x_\beta \end{bmatrix}. \quad (\text{A.4})$$

Using the matrix notation transformations can be written as

$$\mathbf{x}_{\alpha\beta} = \frac{2}{3} \mathbf{C} \mathbf{x}_{abc} \quad \text{and} \quad \mathbf{x}_{abc} = \mathbf{C}^T \mathbf{x}_{\alpha\beta}, \quad (\text{A.5})$$

where

$$\mathbf{C} = \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \quad (\text{A.6})$$

If the zero sequence is neglected, the three-phase quantity can be represented by a single complex space-vector. The transformation from phase quantities to space vector form and its inverse transformation to is can be given by

$$\underline{x} = x_\alpha + jx_\beta = \frac{2}{3} \left(x_a + e^{j\frac{2\pi}{3}} x_b + e^{-j\frac{2\pi}{3}} x_c \right). \quad (\text{A.7})$$

and

$$\begin{aligned} x_a &= \text{Re}\{\underline{x}\} \\ x_b &= \text{Re}\{\underline{x}e^{-j\frac{2\pi}{3}}\} \\ x_c &= \text{Re}\{\underline{x}e^{j\frac{2\pi}{3}}\}. \end{aligned} \quad (\text{A.8})$$

Direct-quadrature -frame representation of three-phase signals

The simplified Park's transformation given in (A.9) defines the three-phase quantities in reference frame rotating at the angular frequency of ω_s . As the zero sequence is neglected, the transformation is valid only in three-phase three-wire system. The inverse transformation is given in (A.10).

$$\begin{bmatrix} x_d \\ x_q \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos \omega_s t & \cos \left(\omega_s t - \frac{2\pi}{3} \right) & \cos \left(\omega_s t + \frac{2\pi}{3} \right) \\ -\sin \omega_s t & -\sin \left(\omega_s t - \frac{2\pi}{3} \right) & -\sin \left(\omega_s t + \frac{2\pi}{3} \right) \end{bmatrix} \begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} \quad (\text{A.9})$$

$$\begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} = \begin{bmatrix} \cos \omega_s t & -\sin \omega_s t \\ \cos \left(\omega_s t - \frac{2\pi}{3} \right) & -\sin \left(\omega_s t - \frac{2\pi}{3} \right) \\ \cos \left(\omega_s t + \frac{2\pi}{3} \right) & -\sin \left(\omega_s t + \frac{2\pi}{3} \right) \end{bmatrix} \begin{bmatrix} x_d \\ x_q \end{bmatrix} \quad (\text{A.10})$$

Often, of interest is the transformation between the alpha-beta frame and the rotating direct-quadrature-reference frame. The transformation between these two coordinate system and its inversion can be given by

$$\begin{bmatrix} x_d \\ x_q \end{bmatrix} = \begin{bmatrix} \cos \omega_s t & \sin \omega_s t \\ -\sin \omega_s t & \cos \omega_s t \end{bmatrix} \begin{bmatrix} x_\alpha \\ x_\beta \end{bmatrix} \quad (\text{A.11})$$

and

$$\begin{bmatrix} x_\alpha \\ x_\beta \end{bmatrix} = \begin{bmatrix} \cos \omega_s t & -\sin \omega_s t \\ \sin \omega_s t & \cos \omega_s t \end{bmatrix} \begin{bmatrix} x_d \\ x_q \end{bmatrix} \quad (\text{A.12})$$

The latter can be expressed using space vector by

$$\underline{x}^s = \underline{x}e^{-j\omega_s t} \quad (\text{A.13})$$

and

$$\underline{x} = \underline{x}^s e^{j\omega_s t}. \quad (\text{A.14})$$

B TRANSFER FUNCTIONS OF A VOLTAGE-FED VSI-BASED INVERTER

Transfer functions associated to the d-component of the output current of the voltage-fed VSI-type inverter analyzed in Chapter 2 can be given by

$$G_{io-d} = \frac{\hat{i}_{o-d}}{\hat{u}_{dc}} = \frac{1}{sL + r_L} \frac{1}{1 + \frac{\omega_s^2 L^2}{(sL + r_L)^2}} \left(\frac{D_d(sL + r_L) + D_q \omega_s L}{sL + r_L} \right) \quad (B.1)$$

$$Y_{o-d} = -\frac{\hat{i}_{o-d}}{\hat{u}_{o-d}} = \frac{1}{sL + r_L + \frac{\omega_s^2 L^2}{sL + r_L}} = \frac{1}{sL + r_L} \frac{1}{1 + \frac{\omega_s^2 L^2}{(sL + r_L)^2}} \quad (B.2)$$

$$Y_{o-qd} = -\frac{\hat{i}_{o-d}}{\hat{u}_{o-q}} = \frac{1}{sL + r_L + \frac{\omega_s^2 L^2}{sL + r_L}} \frac{\omega_s L}{sL + r_L} = \frac{1}{sL + r_L} \frac{1}{1 + \frac{\omega_s^2 L^2}{(sL + r_L)^2}} \frac{\omega_s L}{sL + r_L} \quad (B.3)$$

$$G_{co-d} = \frac{\hat{i}_{o-d}}{\hat{d}_d} = \frac{1}{sL + r_L + \frac{\omega_s^2 L^2}{sL + r_L}} U_{dc} = \frac{1}{sL + r_L} \frac{1}{1 + \frac{\omega_s^2 L^2}{(sL + r_L)^2}} U_{dc} \quad (B.4)$$

$$G_{co-qd} = \frac{\hat{i}_{o-d}}{\hat{d}_q} = \frac{1}{sL + r_L + \frac{\omega_s^2 L^2}{sL + r_L}} \frac{\omega_s L U_{dc}}{sL + r_L} = \frac{1}{sL + r_L} \frac{1}{1 + \frac{\omega_s^2 L^2}{(sL + r_L)^2}} \frac{\omega_s L}{sL + r_L} U_{dc} \quad (B.5)$$

Transfer functions associated to the q-component of the voltage-fed VSI-type inverter output current can be given by

$$G_{io-q} = \frac{\hat{i}_{o-q}}{\hat{u}_{dc}} = \frac{1}{sL + r_L + \frac{\omega_s^2 L^2}{sL + r_L}} \left(\frac{D_q(sL + r_L) - D_d \omega_s L}{sL + r_L} \right) \quad (B.6)$$

$$Y_{o-dq} = -\frac{\hat{i}_{o-q}}{\hat{u}_{o-d}} = -\frac{1}{sL + r_L + \frac{\omega_s^2 L^2}{sL + r_L}} \frac{\omega_s L}{sL + r_L} = -\frac{1}{sL + r_L} \frac{1}{1 + \frac{\omega_s^2 L^2}{(sL + r_L)^2}} \frac{\omega_s L}{sL + r_L} \quad (B.7)$$

$$Y_{o-q} = -\frac{\hat{i}_{o-q}}{\hat{u}_{o-q}} = \frac{1}{sL + r_L + \frac{\omega_s^2 L^2}{sL + r_L}} = \frac{1}{sL + r_L} \frac{1}{1 + \frac{\omega_s^2 L^2}{(sL + r_L)^2}} \quad (B.8)$$

$$G_{co-dq} = \frac{\hat{i}_{o-q}}{\hat{d}_d} = -\frac{1}{sL + r_L + \frac{\omega_s^2 L^2}{sL + r_L}} \frac{\omega_s L U_{dc}}{sL + r_L} = -\frac{1}{sL + r_L} \frac{1}{1 + \frac{\omega_s^2 L^2}{(sL + r_L)^2}} \frac{\omega_s L}{sL + r_L} U_{dc} \quad (B.9)$$

$$G_{co-q} = \frac{\hat{i}_{o-q}}{\hat{d}_q} = \frac{1}{sL + r_L + \frac{\omega_s^2 L^2}{sL + r_L}} U_{dc} = \frac{1}{sL + r_L} \frac{1}{1 + \frac{\omega_s^2 L^2}{(sL + r_L)^2}} U_{dc} \quad (B.10)$$

Transfer functions associated to the input terminal of the voltage-fed VSI-type inverter can be given by

$$Y_{\text{in}} = \frac{\hat{i}_{\text{dc}}}{\hat{u}_{\text{dc}}} = \frac{1}{sL + r_L + \frac{\omega_s^2 L^2}{sL + r_L}} \left(\frac{3D_d}{2} \frac{D_d(sL + r_L) + D_q \omega_s L}{sL + r_L} + \frac{3D_q}{2} \frac{D_q(sL + r_L) - D_d \omega_s L}{sL + r_L} \right) \quad (\text{B.11})$$

$$T_{\text{oi-d}} = \frac{\hat{i}_{\text{dc}}}{\hat{u}_{\text{o-d}}} = -\frac{1}{sL + r_L} \frac{1}{1 + \frac{\omega_s^2 L^2}{(sL + r_L)^2}} \left(\frac{3}{2} D_d - \frac{3}{2} D_q \frac{\omega_s L}{sL + r_L} \right) \quad (\text{B.12})$$

$$T_{\text{oi-q}} = \frac{\hat{i}_{\text{dc}}}{\hat{u}_{\text{o-q}}} = -\frac{1}{sL + r_L} \frac{1}{1 + \frac{\omega_s^2 L^2}{(sL + r_L)^2}} \left(\frac{3}{2} D_q + \frac{3}{2} D_d \frac{\omega_s L}{sL + r_L} \right) \quad (\text{B.13})$$

$$G_{\text{ci-d}} = \frac{\hat{i}_{\text{dc}}}{\hat{d}_d} = \frac{1}{sL + r_L} \frac{1}{1 + \frac{\omega_s^2 L^2}{(sL + r_L)^2}} \left(\frac{3D_d}{2} U_{\text{dc}} + \frac{3D_q}{2} \frac{\omega_s L}{sL + r_L} U_{\text{dc}} \right) + \frac{3I_{\text{o-d}}}{2} \quad (\text{B.14})$$

$$G_{\text{ci-q}} = \frac{\hat{i}_{\text{dc}}}{\hat{d}_q} = \frac{1}{sL + r_L} \frac{1}{1 + \frac{\omega_s^2 L^2}{(sL + r_L)^2}} \left(\frac{3D_q}{2} U_{\text{dc}} + \frac{3D_d}{2} \frac{\omega_s L}{sL + r_L} U_{\text{dc}} \right) + \frac{3I_{\text{o-q}}}{2} \quad (\text{B.15})$$

C TRANSFER FUNCTIONS OF A TWO-STAGE INVERTER VOLTAGE-BOOSTING STAGE

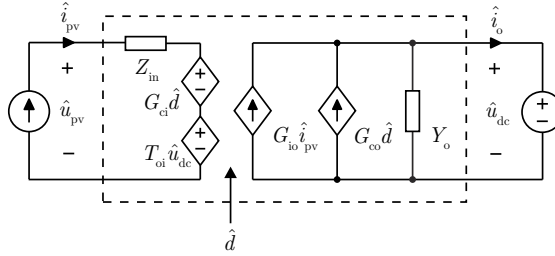


Figure C.1. Linear model of a voltage-boosting converter

The linear model and transfer functions associated to two-stage inverter voltage-boosting stage shown in Fig. C.1 can be given by

$$\begin{bmatrix} \hat{u}_{pv} \\ \hat{i}_o \end{bmatrix} = \begin{bmatrix} Z_{in} & T_{oi} & G_{ci} \\ G_{io} & -Z_o & G_{co} \end{bmatrix} \begin{bmatrix} \hat{i}_{pv} \\ \hat{u}_{dc} \\ \hat{d} \end{bmatrix}, \quad (C.1)$$

$$Z_{in} = \frac{1}{\Delta} \frac{(L_1 s + R_1 - r_{Cin})(r_{Cin} C_{in} s + 1)}{L_1 C_{in}} \quad (C.2)$$

$$T_{oi} = \frac{1}{\Delta} \frac{D'(r_{Cin} C_{in} s + 1)}{L_1 C_{in}} \quad (C.3)$$

$$G_{ci} = -\frac{1}{\Delta} \frac{(U_{dc} + U_D)(r_{Cin} C_{in} s + 1)}{L_1 C_{in}} \quad (C.4)$$

$$G_{io} = \frac{1}{\Delta} \frac{D'(r_{Cin} C_{in} s + 1)}{L_1 C_{in}} \quad (C.5)$$

$$Y_o = \frac{1}{\Delta} \frac{D'^2 s}{L} \quad (C.6)$$

$$G_{co} = \frac{1}{\Delta} I_{pv} \left(s^2 - \frac{1}{L_1} \left(\frac{D'(U_{dc} + U_D)}{I_{pv}} - R_1 \right) s - \frac{1}{L_1 C_{in}} \right), \quad (C.7)$$

where characteristic polynomial and the coefficient R_1 are

$$\Delta = s^2 + \frac{R_1}{L_1}s + \frac{1}{L_1C_{in}} \quad (C.8)$$

and

$$R_1 = r_L + r_{Cin} + Dr_{sw} + D'r_D. \quad (C.9)$$

The steady state operating point of the converter can be given by

$$D = \frac{U_{dc} - U_{pv} + (r_L + r_D)I_{pv} + U_D}{U_{dc} - (r_{sw1} - r_D)I_{pv} + U_D} \quad (C.10)$$

$$I_o = D'I_{pv}, \quad U_{Cin} = U_{pv} \quad \text{and} \quad I_L = I_{pv}. \quad (C.11)$$

Source effect

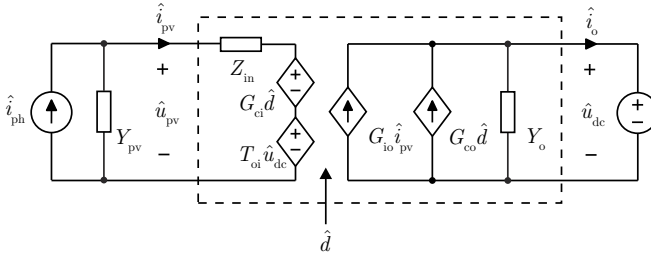


Figure C.2. Linear model with non-ideal source.

$$\begin{bmatrix} \hat{u}_{pv} \\ \hat{i}_o \end{bmatrix} = \begin{bmatrix} Z_{in}^S & T_{oi}^S & G_{ci}^S \\ G_{io}^S & -Y_o^S & G_{co}^S \end{bmatrix} \begin{bmatrix} \hat{i}_{ph} \\ \hat{u}_{dc} \\ \hat{d} \end{bmatrix}, \quad (C.12)$$

$$Z_{in}^S = \frac{Z_{in}}{1 + Y_{pv}Z_{in}} \quad (C.13)$$

$$T_{oi}^S = \frac{T_{oi}}{1 + Y_{pv}Z_{in}} \quad (C.14)$$

$$G_{ci}^S = \frac{G_{ci}}{1 + Y_{pv}Z_{in}} \quad (C.15)$$

$$G_{io}^S = \frac{G_{io}}{1 + Y_{pv}Z_{in}} \quad (C.16)$$

$$Y_o^S = \frac{1 + Y_{pv}Z_{in-oco}}{1 + Y_{pv}Z_{in}} Y_o \quad (C.17)$$

$$G_{co}^S = \frac{1 + Y_{pv}Z_{in-\infty}}{1 + Y_{pv}Z_{in}} G_{co} \quad (C.18)$$

where

$$Z_{in-oco} = Z_{in} + \frac{T_{oi}G_{io}}{Y_o} \quad \text{and} \quad Z_{in-\infty} = Z_{in} - \frac{G_{io}G_{ci}}{G_{co}}. \quad (C.19)$$

Input voltage control

$$\begin{bmatrix} \hat{u}_{pv} \\ \hat{i}_o \end{bmatrix} = \begin{bmatrix} Z_{in}^{inS} & T_{oi}^{inS} & G_{ci}^{inS} \\ G_{io}^{inS} & -Y_o^{inS} & G_{co}^{inS} \end{bmatrix} \begin{bmatrix} \hat{i}_{ph} \\ \hat{u}_{dc} \\ \hat{u}_{pv}^{ref} \end{bmatrix}, \quad (C.20)$$

Assuming unity the measurement gain, the closed-loop transfer functions of the boost-stage can be given by

$$Z_{in}^{inS} = \frac{1}{1 + L^{in}} Z_{in}^S \quad (C.21)$$

$$T_{oi}^{inS} = \frac{1}{1 + L^{in}} Z_{in}^S \quad (C.22)$$

$$G_{ci}^{inS} = \frac{L^{in}}{1 + L^{in}} \quad (C.23)$$

$$G_{io}^{inS} = \frac{G_{io}^S}{1 + L^{in}} + \frac{L^{in}}{1 + L^{in}} G_{io-\infty} \quad (C.24)$$

$$Y_o^{inS} = \frac{1}{1 + L^{in}} Y_o^S + \frac{L^{in}}{1 + L^{in}} Y_{o-\infty} \quad (C.25)$$

$$G_{co}^{inS} = \frac{G_{co}^S}{G_{ci}^S} \frac{1}{1 + L^{in}} \quad (C.26)$$

where

$$G_{io-\infty} = G_{io} - \frac{G_{co} Z_{in}}{G_{ci}}, \quad Y_{o-\infty} = Y_o + \frac{G_{co} T_{oi}}{G_{ci}}, \quad L_{in} = G_{ci}^S G_{pwm} G_c^{uin} \quad (C.27)$$

and G_c^{uin} the input voltage controller transfer function.

D LABORATORY SETUP

The parameters of the designed prototype converter are summarized in Table D.1. The control system and the space-vector modulator was implemented in a digital signal processor TMS320F28335 manufactured by Texas Instruments. The switching frequency of the converter and the digital control system sampling time were 75 kHz and 13.333 μ s, respectively.

Table D.1. Prototype converter parameters.

C_1, C_2	L_1, L_2	C_{in}	L	U_D
220 μ F	200 μ H	100 μ F	200 mH	0.2 V
r_{C1}, r_{C2}	r_{L1}, r_{L2}	r_{Cin}	$r_L + r_{sw}$	r_D
200 m Ω	200 m Ω	30 m Ω	30 m Ω	50 m Ω

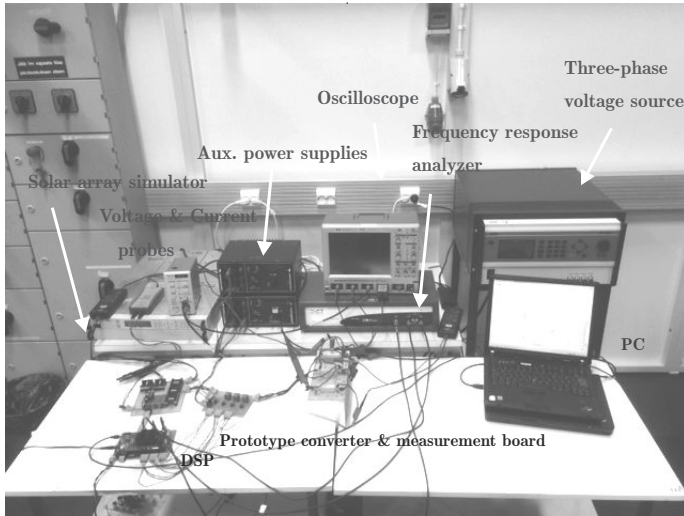


Figure D.1. Overview of the laboratory setup.

Implementation of space-vector modulator using DSP

The space-vector-based algorithm used to insert the shoot-through states inside the switching sequence is given below.

// The reference duty ratio (components d_{α} , d_{β} , d_{st}) is given by
 // the control system of the inverter. Assuming that reference is in sector 1

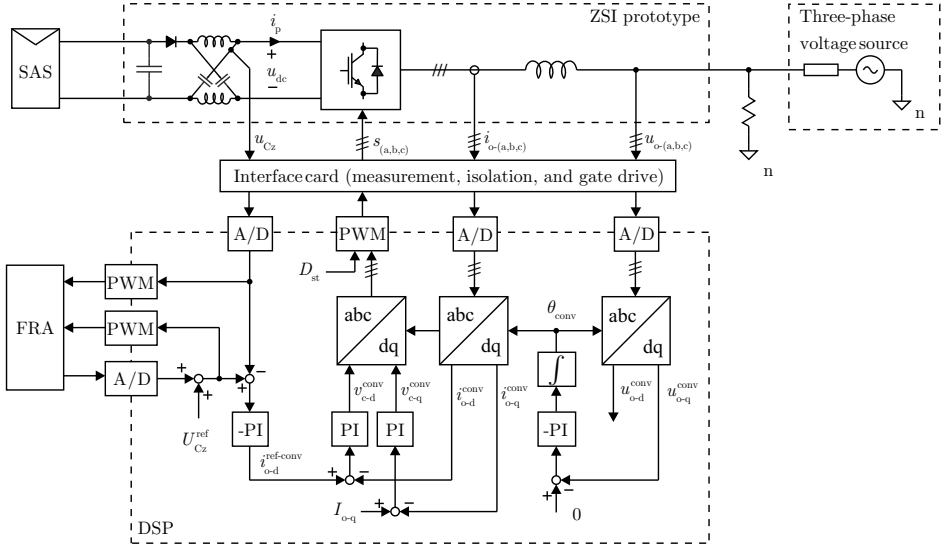


Figure D.2. The configuration used for the loop-gain measurement. The resistive load was inserted between the inverter and the three-phase source due to hardware limitations.

```

d_11 = 1.5*d_alpha - 1.5/sqrt(3.0)*d_beta;    d_12 = 2.0*1.5/sqrt(3.0)*d_beta;
// Assuming that reference is in sector 2
d_22 = 1.5*d_alpha + 1.5/sqrt(3.0)*d_beta;    d_23 = -d_11;
// Assuming that reference is in sector 3
d_33 = d_12;    d_34 = -d_22;
// Determine the reference duty ratio sector and set PWM duty ratios
// (6 channel PWM required) to obtain the correct switching sequence.
if ( d_11 * d_12 > 0 ) {
    if ( d_11 > 0 ) {
        // Reference duty ratio is in sector 1. Switching sequence is 8,2,1,7 and
        // 1/3 of the shoot-through length is added between the switching states
        // Zero states are divided equally at the beginning and end of sequence
        d_zero = 0.5*(1 - d_11 - d_12 - d_st);
        d_ap = 1.0000 - d_zero;    d_an = d_ap - 0.333*d_st;
        d_bp = d_an - d_11;    d_bn = d_bp - 0.333*d_st;
        d_cp = d_zero + 0.333*d_st;    d_cn = d_zero;
    } else {
        // Reference is in sector 4 - sequence: 8,4,5,7
        d_zero = 0.5*(1 + d_11 + d_12 - d_st);
        d_cp = 1.0000 - d_zero;    d_cn = d_cp - 0.333*d_st;
        d_bp = d_cn + d_12;    d_bn = d_bp - 0.333*d_st;
        d_ap = d_zero + 0.333*d_st;    d_an = d_zero;
    }
} else if ( d_22 * d_23 > 0 ) {
    if ( d_22 > 0 ) {
        // Reference is in sector 2 - sequence: 8,2,3,7
        d_zero = 0.5*(1 - d_23 - d_22 - d_st);
        d_bp = 1.0000 - d_zero;    d_bn = d_bp - 0.333*d_st;
        d_ap = d_bn - d_23;    d_an = d_ap - 0.333*d_st;
        d_cp = d_zero + 0.333*d_st;    d_cn = d_zero;
    } else {
        // Reference is in sector 5 - sequence: 8,6,5,7

```



```

    d_zero = 0.5*(1 + d_23 + d_22 - d_st);
    d_cp = 1.0000 - d_zero;          d_cn = d_cp - 0.333*d_st;
    d_ap = d_cn + d_22;              d_an = d_ap - 0.333*d_st;
    d_bp = d_zero + 0.333*d_st;      d_bn = d_zero;
}
} else if ( d_33 > 0 ) {
// Reference is in sector 3 - sequence: 8,4,3,7
d_zero = 0.5*(1 - d_34 - d_33 - d_st);
d_bp = 1.0000 - d_zero;          d_bn = d_bp - 0.333*d_st;
d_cp = d_bn - d_33;              d_cn = d_cp - 0.333*d_st;
d_ap = d_zero + 0.333*d_st;      d_an = d_zero;
} else {
// Reference is in sector 6 - sequence: 8,6,1,7
d_zero = 0.5*(1 + d_34 + d_33 - d_st);
d_ap = 1.0000 - d_zero;          d_an = d_ap - 0.333*d_st;
d_cp = d_an + d_34;              d_cn = d_cp - 0.333*d_st;
d_bp = d_zero + 0.333*d_st;      d_bn = d_zero;
}
}

```

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